Two-Channel, 2.75kV_{RMS} I²C Isolator

General Description

The MAX14933 is a two-channel, 2.75kV_{RMS} I²C digital isolator utilizing Maxim's proprietary process technology. For applications requiring 5kV_{RMS} of isolation, refer to the MAX14937 data sheet. The MAX14933 transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The device offers two bidirectional, open-drain channels for applications, such as I²C, that require data to be transmitted in both directions on the same line. To prevent latch-up action, the A-side outputs comprise special buffers that regulate the logic-low voltage at 0.9V (max), and the input logic-low threshold is at least 50mV lower than the output logic-low voltage. The B side features conventional buffers that do not regulate logic-low output voltage.

The device features independent 2.25V to 5.5V supplies on each side of the isolator. The device operates from DC to 1.7MHz and can be used in isolated I²C busses with clock stretching.

The MAX14933 is available in both a 16-pin wide-body (10.3mm x 7.5mm) and narrow-body (9.9mm x 3.9mm) SOIC package. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

Applications

- I²C, SMBus, PMBus[™] Interfaces
- Power Supplies
- **Battery Management**
- Instrumentation

Functional Diagram



PMBus is a trademark of SMIF. Inc.



Benefits and Features

- Robust Galvanic Isolation of Digital Signals
- Withstands 2.75kV_{RMS} for 60s (V_{ISO})
- Continuously Withstands 443V_{RMS} (V_{IOWM})
- 630V_{PEAK} Repetitive Peak Voltage (V_{IORM})
- Withstands ±10kV Surge per IEC 61000-4-5
- 2 Packages (4mm or 8mm Creepage and Clearance)
- Interfaces Directly with Most Micros and FPGAs Accepts 2.25V to 5.5V Supplies
 - · Bidirectional Data Transfer from DC to 1.7MHz
- Low Power Consumption
 - 5.3mA per Channel Typical at 1.7MHz

Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-10

Ordering Information appears at end of data sheet.

Two-Channel, 2.75kV_{RMS} I²C Isolator

Absolute Maximum Ratings

V _{DDA} to GNDA	0.3V to +6V
V _{DDB} to GNDB	0.3V to +6V
I/OA_ to GNDA	0.3V to +6V
I/OB_ to GNDB	0.3V to +6V
Short-Circuit Duration	
(I/OA_ to GNDA, I/OB_ to GNDB)	Continuous

Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
Wide SO (derate 14.1mW/ºC above +70°C).	1126.8mW
Narrow SO (derate 20mW/°C above +70°C).	1600mW
Operating Temperature Range	-40°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 Wide SOIC

Package Code	W16M+8			
Outline Number	21-0042			
Land Pattern Number	90-0107			
THERMAL RESISTANCE, FOUR-LAYER BOARD				
Junction to Ambient (θ_{JA})	71°C/W			
Junction to Case (θ_{JC})	23°C/W			
16 Narrow SOIC				
Package Code	S16M+11			
Outline Number	<u>21-0041</u>			
Land Pattern Number	90-0442			
THERMAL RESISTANCE, FOUR-LAYER BOARD				
Junction to Ambient (θ_{JA})	50°C/W			
Junction to Case (θ_{JC})	8°C/W			

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

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DC Electrical Characteristics

 $(V_{DDA} - V_{GNDA} = +2.25V \text{ to } +5.5V, V_{DDB} - V_{GNDB} = +2.25V \text{ to } +5.5V, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted}. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25^{\circ}\text{C}, \text{ unless otherwise noted}.) (Note 1) (Note 2)$

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
	V _{DDA}	Relative to GNDA		2.25		5.5	V
Operating Supply voltage	V _{DDB}	Relative to GNDB		2.25		5.5	V
Undervoltage-Lockout Threshold	V _{UVLO} _	V _{DD} rising		1.7	2.0	2.2	V
Undervoltage-Lockout Threshold Hysteresis	V _{UVLO} _ HYST				85		mV
			V _{DDA} = 5V		6	9	
	I _{DDA}	Side A, all channels DC or	V _{DDA} = 3.3V		6	9	
Supply Current			V _{DDA} = 2.5V		5.9	9	mΔ
		Cide D, ell sherrede DC en	V _{DDB} = 5V		4.8	8	
	I _{DDB}	Side B, all channels DC or 1.7MHz	V _{DDB} = 3.3V		4.8	8	-
			V _{DDB} = 2.5V		4.7	8	
Static Output Loading	I _{I/OA} _	Side A	0.5		3	mΔ	
	I _{I/OB} _	Side B	0.5		30		
LOGIC INPUTS AND OUTPUTS							
	V _{IH}	V _{I/OA} _ relative to GNDA	0.7				
Input High Voltage		V _{I/OB} _ relative to GNDB	0.7 x V _{DDB}			V	
		V _{I/OA} _ relative to GNDA			0.5		
Input Low Voltage	VIL	V _{I/OB} _ relative to GNDB			0.3 x V _{DDB}	V	
Input/Output Logic-Low Level Difference	DVI/OL	I _{/OA_} (Note 3), V _{OL} - V _{IL}		50			mV
		$V_{I/OA}$ relative to GNDA, $I_{I/OA}$ = 3mA sink		600		900	
Output Voltage Low	V _{OL}	$V_{I/OA}$ relative to GNDA, $I_{I/OA}$ = 0.5mA sink		600		850	mV
		$V_{I/OB}$ relative to GNDB, $I_{I/OB}$ = 30mA sink				400	
Leakage Current	١L	$I/OA_ = V_{DDA}, I/OB_ = V_{DDB}$	-1		+1	μA	
Input Capacitance	C _{IN}	I/OA_, I/OB_, f = 1MHz			5		pF

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Dynamic Characteristics

 $(V_{DDA} - V_{GNDA} = +2.25V \text{ to } +5.5V, V_{DDB} - V_{GNDB} = +2.25V \text{ to } +5.5V, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted}. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25^{\circ}\text{C}, \text{ unless otherwise noted}.) (Note 4)$

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	$IN_ = GND_ or V_D$	_{D_} (Note 5)		25		kV/µs
Maximum Frequency	f _{MAX}					1.7	MHz
			$4.5V \le V_{DDA}, V_{DDB} \le 5.5V,$ $C_{LA} = 40pF, R_A = 1.6k\Omega,$ $C_{LB} = 400pF, R_B = 180\Omega$			80	
	t _{FA}	I/OA_ = 0.9V _{DDA} to 0.9V	$\begin{array}{l} 3.0V \leq V_{DDA}, V_{DDB} \leq 3.6V, \\ C_{LA} = 40 \text{pF}, \ \text{R}_{\text{A}} = 1 \text{k}\Omega, \\ C_{\text{LB}} = 400 \text{pF}, \ \text{R}_{\text{B}} = 120\Omega \end{array}$			65	
Foll Time (Figure 1)			$2.25V \le V_{DDA}, V_{DDB} \le 2.75V,$ $C_{LA} = 40pF, R_A = 810\Omega,$ $C_{LB} = 400pF, R_B = 91\Omega$			55	20
			$4.5V \le V_{DDA}, V_{DDB} \le 5.5V,$ $C_{LA} = 40pF, R_A = 1.6k\Omega,$ $C_{LB} = 400pF, R_B = 180\Omega$			35	115
	t _{FB}	I/OB_ = 0.9V _{DDB} to 0.1V _{DDB}	$\begin{array}{l} 3.0V \leq V_{DDA}, V_{DDB} \leq 3.6V, \\ C_{LA} = 40 \text{pF}, \ \text{R}_{\text{A}} = 1 \text{k}\Omega, \\ C_{\text{LB}} = 400 \text{pF}, \ \text{R}_{\text{B}} = 120\Omega \end{array}$			45	-
			$\begin{array}{l} 2.25 V \leq V_{DDA}, V_{DDB} \leq 2.75 V, \\ C_{LA} = 40 \text{pF}, \ \text{R}_{\text{A}} = 810 \text{k}\Omega, \\ C_{\text{LB}} = 400 \text{pF}, \ \text{R}_{\text{B}} = 91 \Omega \end{array}$			75	
	^t PLHAB	I/OA_ = 0.5V _{DDA} to I/OB_ = 0.7V _{DDB}	$\begin{array}{l} 4.5V \leq V_{DDA}, V_{DDB} \leq 5.5V, \\ C_{LA} = 0pF, R_A = 1.6k\Omega, \\ C_{LB} = 0pF, R_B = 180\Omega \end{array}$			20	
Propagation Delay (Figure 1)			$\begin{array}{l} 3.0V \leq V_{DDA}, V_{DDB} \leq 3.6V, \\ C_{LA} = 0pF, R_A = 1k\Omega, \\ C_{LB} = 0pF, R_B = 120\Omega \end{array}$			25	
			$\begin{array}{l} 2.25 V \leq V_{DDA}, V_{DDB} \leq 2.75 V, \\ C_{LA} = 0 p F, R_A = 810 \Omega, \\ C_{LB} = 0 p F, R_B = 91 \Omega \end{array}$			35	20
	t _{PHLAB} ^t PHLAB to I/OB_ = 0.4V		$\begin{array}{l} 4.5V \leq V_{DDA}, V_{DDB} \leq 5.5V, \\ C_{LA} = 0pF, R_A = 1.6k\Omega, \\ C_{LB} = 0pF, R_B = 180\Omega \end{array}$			80	115
		I/OA_ = 0.5V _{DDA} to I/OB_ = 0.4V	$\begin{array}{l} 3.0V \leq V_{DDA}, V_{DDB} \leq 3.6V, \\ C_{LA} = 0pF, R_A = 1k\Omega, \\ C_{LB} = 0pF, R_B = 120\Omega \end{array}$			95	
			$\begin{array}{l} 2.25 V \leq V_{DDA}, V_{DDB} \leq 2.75 V, \\ C_{LA} = 0 p F, R_A = 810 \Omega, \\ C_{LB} = 0 p F, R_B = 91 \Omega \end{array}$			110	

Dynamic Characteristics (continued)

 $(V_{DDA} - V_{GNDA} = +2.25V \text{ to } +5.5V, V_{DDB} - V_{GNDB} = +2.25V \text{ to } +5.5V, T_A = -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25^{\circ}\text{C}, \text{ unless otherwise noted.} \text{ (Note 4)}$

PARAMETER	SYMBOL		CONDITIONS	MIN	ТҮР	MAX	UNITS
			$\begin{array}{l} 4.5V\leqV_{DDA},V_{DDB}\leq5.5V,\\ C_{LA}=0pF,R_{A}=1.6k\Omega,\\ C_{LB}=0pF,R_{B}=180\Omega \end{array}$			25	- ns
	^t PLHBA	I/OB_ = 0.5V _{DDB} to I/OA_ = 0.7V _{DDA}	$\begin{array}{l} 3.0V \leq V_{DDA}, \ V_{DDB} \leq 3.6V, \\ C_{LA} = 0pF, \ R_{A} = 1k\Omega, \\ C_{LB} = 0pF, \ R_{B} = 120\Omega \end{array}$			25	
Propagation Dalay (Figure 1)			$\begin{array}{l} 2.25 V \leq V_{DDA}, V_{DDB} \leq 2.75 V, \\ C_{LA} = 0 pF, R_{A} = 810 \Omega, \\ C_{LB} = 0 pF, R_{B} = 91 \Omega \end{array}$			35	
Propagation Delay (Figure 1)	^t PHLBA t	I/OB_ = 0.5V _{DDB} to I/OA_ = 0.9V	$\begin{array}{l} 4.5V\leqV_{DDA},V_{DDB}\leq5.5V,\\ C_{LA}=0pF,R_{A}=1.6k\Omega,\\ C_{LB}=0pF,R_{B}=180\Omega \end{array}$			115	
			$\begin{array}{l} 3.0V \leq V_{DDA}, V_{DDB} \leq 3.6V, \\ C_{LA} = 0pF, R_{A} = 1k\Omega, \\ C_{LB} = 0pF, R_{B} = 120\Omega \end{array}$			115	
			2.25V ≤ V_{DDA} , V_{DDB} ≤ 2.75V, C_{LA} = 0pF, R_A = 810Ω, C_{LB} = 0pF, R_B = 91Ω			125	
			$4.5V \le V_{DDA}, V_{DDB} \le 5.5V$			65	
	PWD _{AB}	t _{PLHAB} - t _{PHLAB}	$3.0V \le V_{DDA}, V_{DDB} \le 3.6V$			65	ns
Pulse-Width Distortion			$2.25V \le V_{DDA}, V_{DDB} \le 2.75V$			80	
			$4.5V \le V_{\text{DDA}}, V_{\text{DDB}} \le 5.5V$			95	
	PWD _{BA}	t _{plhba} - t _{phlba}	$3.0V \le V_{DDA}, V_{DDB} \le 3.6V$			95	
			$2.25V \le V_{DDA}, V_{DDB} \le 2.75V$			100	

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human body model, all pins		±4		kV

Note 1: All devices are 100% production tested at $T_A = +125$ °C. Specifications over temperature are guaranteed by design.

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to ground on the corresponding side of the device, unless otherwise noted.

Note 3: This is the minimum difference between the output logic-low level and the input logic threshold. This ensures that there is no possibility of the part latching up the bus to which it is connected.

Note 4: Not production tested. Guaranteed by design.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining operation. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

Safety Regulatory Approvals

UL

The MAX14933 is certified under UL1577. For more details, refer to file E351759.

Rated up to 3750V_{RMS} isolation voltage for single protection.

cUL (EQUIVALENT TO CSA NOTICE 5A)

The MAX14933 are certified up to $3750V_{RMS}$ for single protection. For more details, refer to file E351759.

VDE

The MAX14933 is certified to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12. For details, see file ref. 5015017-4880-0001/217630/EC22/SCT. Basic Insulation, Maximum Transient Isolation Voltage 4600V_{PK}, Maximum Working Voltage 443V_{RMS}

IEC Insulation Testing

 TUV

 The MAX14933 are tested under TUV.

 IEC 60950-1: Up to 630VP (443V_{RMS}) working voltage for basic insulation.

 IEC 61010-1 (ed. 3): Up to 443V_{RMS} working voltage for basic insulation. For details, see Technical Report number 095-72100581-100.

 IEC 60601-1 (ed. 3): For details, see Technical Report number 095-72100581-200.

Basic Insulation 1 MOOP, 630VPK (443V_{RMS})

Withstand Isolation Voltage for 60s (Viso) 2750V_{RMS}

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS	
Partial Discharge Test Voltage	V _{PR}	Method B1 = V _{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	VP	
Maximum Repetitive Peak Isolation Voltage	VIORM		630	VP	
Maximum Working Isolation Voltage	VIOWM		443	V _{RMS}	
Maximum Transient Isolation Voltage	VIOTM	t = 1s	4600	VP	
Maximum Withstand Isolation Voltage	V _{ISO}	f _{SW} = 60Hz, duration = 60s	2750	V _{RMS}	
Maximum Surge Isolation Voltage	VIOSM	Basic insulation 1.2/50µ pulse	10	kV	
Insulation Resistance	R _S	$T_A = +150^{\circ}C$ V _{IO} = 500V	> 10 ¹²	Ω	
Barrier Capacitance Input-to-Output (Note 6)	CIO	f _{SW} = 1MHz	2	pF	
Minimum Croonago Dictoreo	CPC	Wide SOIC	8	mm	
Minimum Creepage Distance	CPG	Narrow SOIC	4	11111	
Minimum Claaranaa Distance		Wide SOIC	8	mm	
	ULK	Narrow SOIC	4		
Internal Clearance		Distance through insulation	0.015	mm	
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575		
Climatic Category			40/125/21		
Pollution Degree (DIN VDE 0110, Table 1)			2		

Note 6: Capacitance is measured with all pins on side A and side B tied together.

Two-Channel, 2.75kV_{RMS} I²C Isolator



Figure 1. Test Circuit (A) and Timing Diagram (B)

Two-Channel, 2.75kV_{RMS} I²C Isolator

Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)



Two-Channel, 2.75kV_{RMS} I²C Isolator

Typical Operating Characteristics (continued) (V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)









Two-Channel, 2.75kV_{RMS} I²C Isolator

Pin Configuration



Pin Description

PIN	NAME	FUNCTION	VOLTAGE RELATIVE TO
1, 7	GNDA	Ground Reference For Side A. Ensure both pins 1 and 7 are connected to GNDA.	_
2, 8	I.C.	Internally Connected. Connect to GNDA or leave unconnected.	GNDA
4, 13	N.C.	No Connection. Not internally connected.	
3	V _{DDA}	Power Supply. Bypass $V_{\mbox{DDA}}$ with a $0.1\mu\mbox{F}$ ceramic capacitor as close as possible to the pin.	GNDA
5	I/OA1	Bidirectional Input/Output 1 On Side A. I/OA1 is translated to/from I/OB1 and is an open-drain output.	GNDA
6	I/OA2	Bidirectional Input/Output 2 On Side A. I/OA2 is translated to/from I/OB2 and is an open-drain output.	GNDA
9, 16	GNDB	Ground Reference For Side B.	—
10, 15	I.C.	Internally Connected. Connect to GNDB or leave unconnected.	GNDB
11	I/OB2	Bidirectional Input/Output 2 On Side B. I/OB2 is translated to/from I/OA2 and is an open-drain output.	GNDB
12	I/OB1	Bidirectional Input/Output 1 On Side B. I/OB1 is translated to/from I/OA1 and is an open-drain output.	GNDB
14	V _{DDB}	Power Supply. Bypass V_{DDB} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDB

Typical Application Circuit



Detailed Description

The MAX14933 is a two-channel, 2.75kV_{RMS} I²C isolator utilizing Maxim's proprietary process technology. For applications requiring $5kV_{RMS}$ of isolation, refer to the MAX14937 data sheet. The device transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The device offers two bidirectional, open-drain channels for applications, such as I^2C , that require data to be transmitted in both directions on the same line.

The device features independent 2.25V to 5.5V supplies on each side of the isolator. The device operates from DC to 1.7MHz and can be used in isolated I²C busses with clock stretching. The wide temperature range and high isolation voltage make the device ideal for use in harsh industrial environments.

Digital Isolation

The device provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to $630V_{PEAK}$ of continuous isolation is supported, as well as transient differences of up to $2.75kV_{RMS}$ for up to 60s.

Bidirectional Channels

The device features two bidirectional channels that have open-drain outputs. The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device. I/OA1 and I/OA2 outputs comprise special buffers that regulate the logic-low voltage at approximately 0.7V. The input logic-low threshold (V_{IL}) of I/OA1 and I/OA2 is at least 50mV lower than the output logic-low voltage of I/OA1 and I/OA2. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B; thus, preventing a latching action. I/OB1 and I/OB2 are conventional outputs that do not regulate the logic-low output voltage.

Due to their nature, the A-side output buffers of the MAX14933 cannot be connected together, or to a device with similar buffers or rise-time accelerators. However, the B-side output buffers of the MAX14933 can be connected together, or to any other bidirectional buffer or level translator.

The I/OA1, I/OA2, I/OB1, and I/OB2 pins have opendrain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 30mA for side B, and 3mA for side A (see the <u>DC Electrical</u> <u>Characteristics</u> table). The device supports I²C clock stretching.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage event is detected on either of the supplies, all bidirectional outputs become high impedance and are pulled high by the external pullup resistor on the open-drain outputs (<u>Table 1</u>). <u>Figure 2</u> through <u>Figure 5</u> shows the behavior of the outputs during power-up and power-down.

Applications Information

Effect of Continuous Isolation on Lifetime

High-voltage conditions cause insulation to degrade over time. Higher voltages result in faster degradation. Even the high-quality insulating material used in the device can degrade over long periods of time with a constant high voltage across the isolation barrier.

Power-Supply Sequencing

The MAX14933 does not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB} . Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1μ F ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close as possible to the power-supply input pins.

Input/Output Capacitive Loads

For optimal performance, ensure that C_{LA} is \leq 40pF and C_{LB} \leq 400pF.

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V _{DDA}	V _{DDB}	V _{I/OA} _	V _{I/OB} _
Powered	Powered	1	1
Powered	Powered	0	0
Undervoltage	Powered	High-Z	Х
Powered	Undervoltage	Х	High-Z

Table 1. Output Behavior During Undervoltage Conditions

X = Don't care.



Figure 2. Undervoltage-Lockout Behavior (I/OB_ Set High)







Figure 3. Undervoltage-Lockout Behavior (I/OA_ Set High)



Figure 5. Undervoltage-Lockout Behavior (I/OA_ Set Low)

Two-Channel, 2.75kV_{RMS} I²C Isolator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14933AWE+	-40°C to +125°C	16 Wide SOIC
MAX14933ASE+	-40°C to +125°C	16 Narrow SOIC

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BICMOS

Two-Channel, 2.75kV_{RMS} I²C Isolator

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/16	Initial release	—
1	5/16	Added IEC Insulation Testing table	1, 6
2	1/17	Removed VDE pending and future product status of MAX14933	6, 14
3	11/19	Updated the General Description, Absolute Maximum Ratings and Package Informa- tion sections, ESD Protection and Safety Regulatory Approvals tables, and replaced the Bidrectional Channels section	1, 12

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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