FEDL62Q1500-04
Issue Date: May 31, 2019

ML62Q1500 Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q1500 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC operator, DMA controller, clock generator, Simplified RTC, timer, UART, synchronous serial port, I^2C bus interface unit, buzzer, Voltage Level Supervisor(VLS), successive approximation type A/D converter, D/A converter , analog comparator, safety function(IEC60730/60335 Class B) and etc.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP(In-System Programming) function supports the Flash programming in production line.
The ML62Q1500 Group has five packages (48pin - 100pin) and ten kinds of memory sizes(32Kbyte - 512Kbyte).

Table 1 ML62Q1500 Group Product List

<table>
<tr><th>Program memory</th><th>Data memory (RAM)</th><th>Data Flash</th><th>48pin
TQFP48</th><th>52pin
TQFP52</th><th>64pin
QFP64
TQFP64</th><th>80pin
QFP80</th><th>100pin
QFP100
TQFP100</th></tr>
<tr><td>512Kbyte</td><td rowspan="2">32Kbyte</td><td rowspan="2">8Kbyte</td><td>–</td><td>–</td><td>ML62Q1559</td><td>ML62Q1569</td><td>ML62Q1579</td></tr>
<tr><td>384Kbyte</td><td>–</td><td>–</td><td>ML62Q1558</td><td>ML62Q1568</td><td>ML62Q1578</td></tr>
<tr><td>256Kbyte</td><td rowspan="3">16Kbyte</td><td rowspan="10">4Kbyte</td><td>–</td><td>–</td><td>ML62Q1557</td><td>ML62Q1567</td><td>ML62Q1577</td></tr>
<tr><td>192Kbyte</td><td>–</td><td>–</td><td>ML62Q1556</td><td>ML62Q1566</td><td>ML62Q1576</td></tr>
<tr><td>160Kbyte</td><td>–</td><td>–</td><td>ML62Q1555</td><td>ML62Q1565</td><td>ML62Q1575</td></tr>
<tr><td rowspan="2">128Kbyte</td><td>16Kbyte</td><td>–</td><td>–</td><td>–</td><td>ML62Q1564</td><td>ML62Q1574</td></tr>
<tr><td>8Kbyte</td><td>ML62Q1534</td><td>ML62Q1544</td><td>ML62Q1554</td><td>–</td><td>–</td></tr>
<tr><td rowspan="2">96Kbyte</td><td>16Kbyte</td><td>–</td><td>–</td><td>–</td><td>ML62Q1563</td><td>ML62Q1573</td></tr>
<tr><td>8Kbyte</td><td>ML62Q1533</td><td>ML62Q1543</td><td>ML62Q1553</td><td>–</td><td>–</td></tr>
<tr><td>64Kbyte</td><td rowspan="3">8Kbyte</td><td>ML62Q1532</td><td>ML62Q1542</td><td>ML62Q1552</td><td>–</td><td>–</td></tr>
<tr><td>48Kbyte</td><td>ML62Q1531</td><td>ML62Q1541</td><td>ML62Q1551</td><td>–</td><td>–</td></tr>
<tr><td>32Kbyte</td><td>ML62Q1530</td><td>ML62Q1540</td><td>ML62Q1550</td><td>–</td><td>–</td></tr>
</table>

FEATURES

- CPU
  - 16-bit RISC CPU : nX-U16/100(A35 core)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-chip debug function built-in (supported by LAPIS on-chip debug emulator EASE1000)
  - ISP (In-System Programming) function built-in
  - Minimum instruction execution time
    30.5 µs (at 32.768 kHz system clock)
    62.5ns/41.6ns (at 16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Multiplication: 16bit × 16bit (operation time 4 cycles)
  - Division: 32bit / 16bit (operation time 8 cycles)
  - Division: 32bit / 32bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

- Operating voltage and temperature
  - Operating voltage: V_{DD} = 1.6 to 5.5 V（Need 1.8V or higher at the power on）
  - Operating temperature: -40 to +105 °C

- Internal memory
  - Program Flash memory area
    Rewrite count: 100 cycles
    Rewrite unit: 32bit(4byte)
    Erase unit: 16Kbyte/1Kbyte
    Erase/Rewrite temperature: 0°C to +40°C

  - Data Flash memory area
    Rewrite count 10,000 cycles
    Rewrite unit: 8bit(1byte)
    Erase unit: all area/128byte
    Erase/Rewrite temperature: -40°C to +85°C
    Back Ground Operation(BGO) : CPU can work while erasing and rewriting.

    This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
    Super Flash® is a registered trademark of Silicon Storage Technology, Inc.

  - Data RAM area
    Rewrite unit: 8bit/16bit(1byte/2byte)
    Parity check function (Parity error reset or interrupt is generatable)

- Clock
  - Low-speed clock
    Internal low-speed RC oscillation: Approx.32.768 kHz
    External low-speed crystal oscillation: 32.768 kHz crystal resonator is connectable
    3 modes is available for the crystal oscillation
    - Tough mode: Largest oscillation allowance to make highest resistance against leakage between the pins
    - Standard mode: Standard oscillation allowance and current consumption
    - Low power current mode: Smaller oscillation allowance than standard mode to make lower current consumption
  - High-speed clock
    PLL oscillation: 24MHz/16MHz is selectable by code option
  - WDT(Watch Dog Timer) clock
    Internal low-speed RC oscillation: Approx. 1kHz
    The WDT independent clock or the divided clock of internal low-speed clock is selectable by the code option.

- Reset
  - RESET_N pin reset
  - Reset by power-on detection
  - Reset by the watchdog timer (WDT) overflow
  - Reset by WDT counter clear during the clear invalid period
  - Reset by RAM parity error
  - Reset by unused ROM access
  - Reset by voltage level detection (VLS)
  - The software reset by BRK instruction (reset CPU only)
  - Reset to the peripheral circuits by Block Reset Control Registers (BRECON 0 to 3)
  - One-time reset to the all peripheral circuits by Software Reset Control Register (SOFTRCON)

- Power management
  - HALT mode: CPU stops executing instruction, clock oscillations and peripheral circuits remain previous states
  - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits working with low-speed clock remain previous states
  - STOP mode: CPU stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
  - STOP-D mode: CPU stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal regulator's output voltage (V_{DDL}) goes down to reduce the current consumption.
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of the oscillation clock)
  - Block Control Function: Powers down the circuits of unused function blocks (reset the block or stop supplying the clock)

- Interrupt controller
  - Non-maskable interrupt source: 1 (Internal sources: WDT)
  - Maskable interrupt sources: max.51 (Internal sources: max.42, External sources: 9)
  - Four step interrupt levels
  - External interrupt ports : max 12

- Watchdog timer(WDT)
  - Operating clock is selectable (1kHz WDT independent clock or divided clock of internal 32.768kHz RC oscillation)
  - Overflow period: 8 types selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2000ms and 8000ms@32.768kHz)
  - Enabling or disabling the window function is selectable (The clear enable period is 50% or 75% of overflow period)
  - WDT operation is selectable by code option (Enable or Disable)
  - Readable WDT counter (WDT counter monitor function)
  - The first overflow generates the WDT interrupt, and the second overflow generates the WDT reset when the counter clear enable period is 100% of overflow period.
  - The first overflow generates the WDT reset when the counter clear enable period is 50% or 75% of overflow period.
  - The invalid clear reset generated when the WDT counter is cleared out of the WDT counter clear enable period.

- DMA(Direct Memory Access) controller
  - Channel: 2ch
  - Transfer unit: 8bit/16bit
  - Max. transfer count: 1024 time
  - Transfer type: 2 cycle transfer
  - Transfer mode: Single transfer mode
    Fixed address, address increments and address decrements
  - Transfer target: SFR/RAM → SFR/RAM (Transfer from/to Flash is not supported)
  - Transfer request: Serial communication units, A/D, 16-bit timers, Functional timers and External interrupts.

- Low-speed Time base counter
  - Divide the Low-speed clock(LSCLK) and generate 128Hz~1Hz internal pulse signals
  - Periodical interrupt × 3 selectable from 8 frequencies (128Hz, 64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz and 1Hz)
  - The time base clock output (1Hz or 2Hz) from general purpose ports (TBCOUT0, TBCOUT1).
  - Built-in frequency adjustment function
    (adjustment range: approx.-488ppm ~ +488ppm, adjustment resolution: approx.0.119ppm)

- Simplified RTC
  - Channel: 1ch
  - Count by one second from "00 min. 00 sec" to "59 min. 59 sec"
  - One interrupt occurrence is selectable from four periodical interrupt requests (0.5sec, 1sec, 30sec or 60sec)
  - Protect function for incorrect writing the minutes and second.

- Functional timer(FTM)
  - Channel: Max. 8ch
  - Repeat mode, Oneshot mode, Capture mode, PWM mode1 and PWM mode 2(complementary output)
  - Same start/stop is available with different channels
    (This function is not available with 16bit General Timer)
  - Event trigger (external interrupts, analog comparators, 16-bit timers and Functional timers)
  - Dead time is generatable.
  - Available to specify division ratio of counter clock channel by channel

- 16-bit timers
  - Channel: Max. 8ch
  - 8-bits timer mode and 16-bit timer mode (1ch 16-bit timer is configurable as 2ch 8-bit timer)
  - Same start/stop is available with different channels
    (This function is not available with Functional Timer)
  - Timer output (toggled by overflow)
  - Available to specify division ratio of counter clock channel by channel

- Serial communication unit
  - Channel: Max. 6ch
  - Synchronous Serial Port or UART is selectable in each channel

  < Synchronous Serial Port >
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

  < UART >
  - Full-duplex communication x 2ch(One Full-duplex UART is configurable as two half-duplex UARTs)
  - 5~8 bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - LSB first/MSB first selectable
  - Wide range of communication speed
    32.768kHz operation clock : 1bps to 4,800bps
    24MHz operation clock : 600bps to 3Mbps
    16MHz operation clock : 300bps to 2Mbps
  - Internal baud rate generator

- I^2C bus interface unit (Master/Slave)
  - Channel: 1ch
  - Master or Slave mode is selectable

  < Master function >
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

  < Slave function >
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Clock stretch function
  - 7bit address format

- I^2C bus interface (Master only)
  - Channel: 2ch
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

- General-purpose ports (GPIO)
  - I/O port: Max. 92 (Including one pin for on-chip debug and pins for other shared functions)
  - Input port: Max. 2(Including a shared function)
  - External interrupt function × 12
  - LED driver port : Max. 91
  - Carrier frequency output function (used for IR communication)

- Successive approximation type A/D converter
  - Channel: Max.16ch
  - Resolution: 10bit
  - Conversion time: Selectable 2.25µs (min) /channel (When the conversion clock is 8MHz)
  - V_{DD}, Internal reference voltage(Approx. 1.55V) or External reference voltage (V_{REF} pin) is selectable.
  - Scan function (repeat conversion)
  - One result register for each channel
  - Interrupt by threshold of conversion result
  - Temperature sensor for low-speed RC oscillation adjustment

- Voltage level supervisor (VLS)
  - Accuracy: ±4%
  - Threshold voltage: 12 values selectable (1.85V ~ 4.00V)
  - Voltage level detection reset (VLS reset)
  - Voltage level detection interrupt (VLS0 interrupt)

- Analog comparator
  - Channel: 2ch
  - Interrupts allow edge selection and sampling selection
  - An external or an internal reference voltage is selectable

- D/A converter
  - Channel: Max 2ch
  - Resolution: 8bit
  - Output impedance: 6k ohm(Typ.)
  - R-2R ladder method

- Buzzer
  - 4 buzzer mode (Repeat sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
  - 8frequencies (4.096kHz to 293Hz)
  - 15 step duty (1/16 to 15/16)
  - Selectable the logic of buzzer output pin (Positive or Negative logic)

- CRC(Cyclic Redundancy Check) operation function
  - Generation equation: $X^{16}+X^{12}+X^5+1$
  - LSB first or MSB first is selectable
  - Automatic CRC mode: Automatic CRC calculation with data of program memory in HALT mode

- Safety Function (IEC60730/60335 Class B)
  - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
  - RAM/SFR guard
  - Automatic CRC calculation with data of program memory
  - RAM parity error detection
  - ROM unused area access reset
  - Clock mutual check
  - WDT counter check
  - Successive approximation type A/D converter test
  - UART test
  - Synchronous serial test
  - I^2C test
  - General port test

- Shipping package
  - 48-pin plastic TQFP
    ML62Q1530/1531/1532/1533/1534 - xxxTB
    （Blank part: ML62Q1530/1531/1532/1533/1534-NNNTB）
  - 52-pin plastic TQFP
    ML62Q1540/1541/1542/1543/1544 - xxxTB
    （Blank part: ML62Q1540/1541/1542/1543/1544-NNNTB）
  - 64-pin plastic TQFP
    ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1558/1559 - xxxTB
    （Blank part: ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1558/1559-NNNTB）
  - 64-pin plastic QFP
    ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1558/1559 - xxxGA
    （Blank part: ML62Q1550/1551/1552/1553/1554/1555/1556/1557/1558/1559-NNNGA）
  - 80-pin plastic QFP
    ML62Q1563/1564/1565/1566/1567 /1568/1569- xxxGA
    （Blank part: ML62Q1563/1564/1565/1566/1567/1568/1569-NNNGA）
  - 100-pin plastic TQFP
    ML62Q1573/1574/1575/1576/1577/1578/1579 - xxxTB
    （Blank part: ML62Q1573/1574/1575/1576/1577/1578/1579-NNNTB）
  - 100-pin plastic QFP
    ML62Q1573/1574/1575/1576/1577/1578/1579 - xxxGA
    （Blank part: ML62Q1573/1574/1575/1576/1577/1578/1579-NNNGA）

xxx: ROM code number

ML62Q1500 Group how to read the part number

ML 62 Q 15 7 7 – xxx TB

- Package Type
  - GA :QFP
  - TB :TQFP
- ROM Code Number
  - NNN :Blank
  - xxx :Custom Code Number
- Program Memory Size
  - 0 :32Kbyte
  - 1 :48Kbyte
  - 2 :64Kbyte
  - 3 :96Kbyte
  - 4 :128Kbyte
  - 5 :160Kbyte
  - 6 :192Kbyte
  - 7 :256Kbyte
  - 8 :384Kbyte
  - 9 :512Kbyte
- Pin Count
  - 3 :48pin
  - 4 :52pin
  - 5 :64pin
  - 6 :80pin
  - 7 :100pin
- Group Name
  - 15 :1500 Group
- Program Memory Type
  - Q :Flash Memory
- CPU Type
  - 62 :16bit CPU nX-U16/100
- LAPIS Semiconductor Logic Product

Figure 1 ML62Q1500 Group Part Number

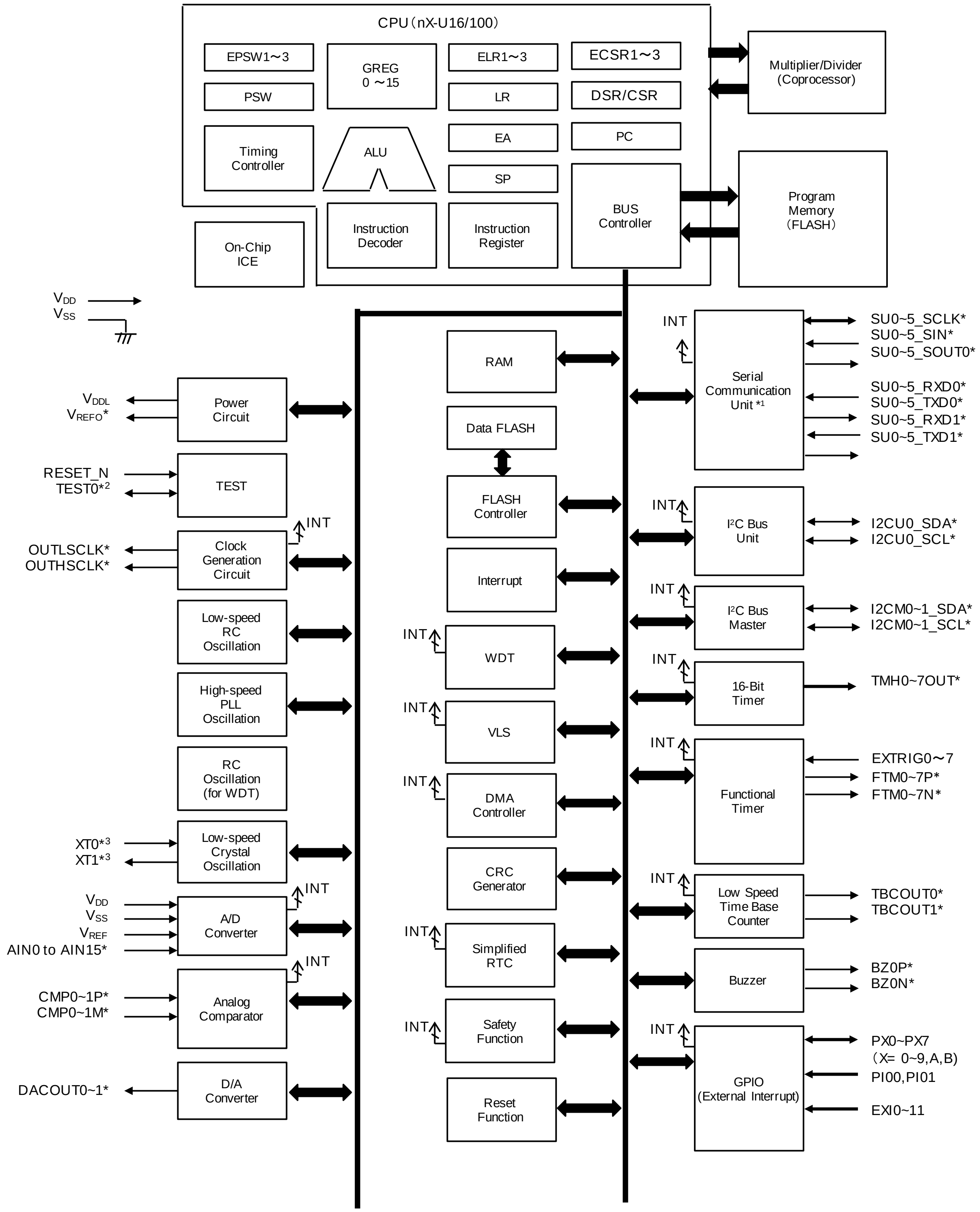
ML62Q1500 Group Main Function List

Table 2 ML62Q1500 Group Main Function List

Part number	Pin						Interrupt		Timer			Serial			Analog			
	Total pin-counts	Power pin counts	Reset Input pin	Input port *3	I/O port	LED drive port	Internal interrupt [source]	External interrupt [port]	Functional Timer [ch]	16bit General I Timer *1 [ch]	Simplified RTC [ch]	Full-duplex UART or Synchronous serial*2 [ch]	I^{2}C bus unit (Master/Slave) [ch]	I^{2}C bus interface (Master only) [ch]	10bit Successive type A/D converter [ch]	Analog comparator [ch]	Analog comparator [input pin]	8bit D/A converter [ch]
ML62Q1530																		
ML62Q1531																		
ML62Q1532	48				42	41												
ML62Q1533																		
ML62Q1534																		
ML62Q1540																		
ML62Q1541																		
ML62Q1542	52				46	45												
ML62Q1543																		
ML62Q1544																		
ML62Q1550		3					31	10	6	6		2			12			1
ML62Q1551																		
ML62Q1552																		
ML62Q1553																		
ML62Q1554	64				58	57												
ML62Q1555																		
ML62Q1556			1	2							1		1	2		2	4	
ML62Q1557																		
ML62Q1558																		
ML62Q1559																		
ML62Q1563																		
ML62Q1564																		
ML62Q1565																		
ML62Q1566	80				72	71												
ML62Q1567																		
ML62Q1568																		
ML62Q1569																		
ML62Q1573		4					43	12	8	8		6			16			2
ML62Q1574																		
ML62Q1575																		
ML62Q1576	100				92	91												
ML62Q1577																		
ML62Q1578																		
ML62Q1579																		

*1 : One 16bit timer is configurable as two 8bit timers
*2 : Full-duplex UART and Synchronous Serial Port can not be used simultaneously in the same channel.
One Full-duplex UART is configurable as two half-duplex UARTs.
*3 : Shared with pins for crystal oscillation

BLOCK DIAGRAM



* : Indicates the shared function of general ports.
*1 : One channel Full-duplex UART is configurable as two channel Half-duplex UART.
*2 : Not available as the input port when connecting to the on-chip debug emulator(EASE1000).
*3 : Not available as the input port when connecting to the crystal resonator.

Figure 2 ML62Q1500 Group Block Diagram

PIN CONFIGURATION

The port names in the pin-layout indicate 1st-function. Refer to Table-3 or Table-4 about other functions.

Pin Layout of 48pin TQFP Package

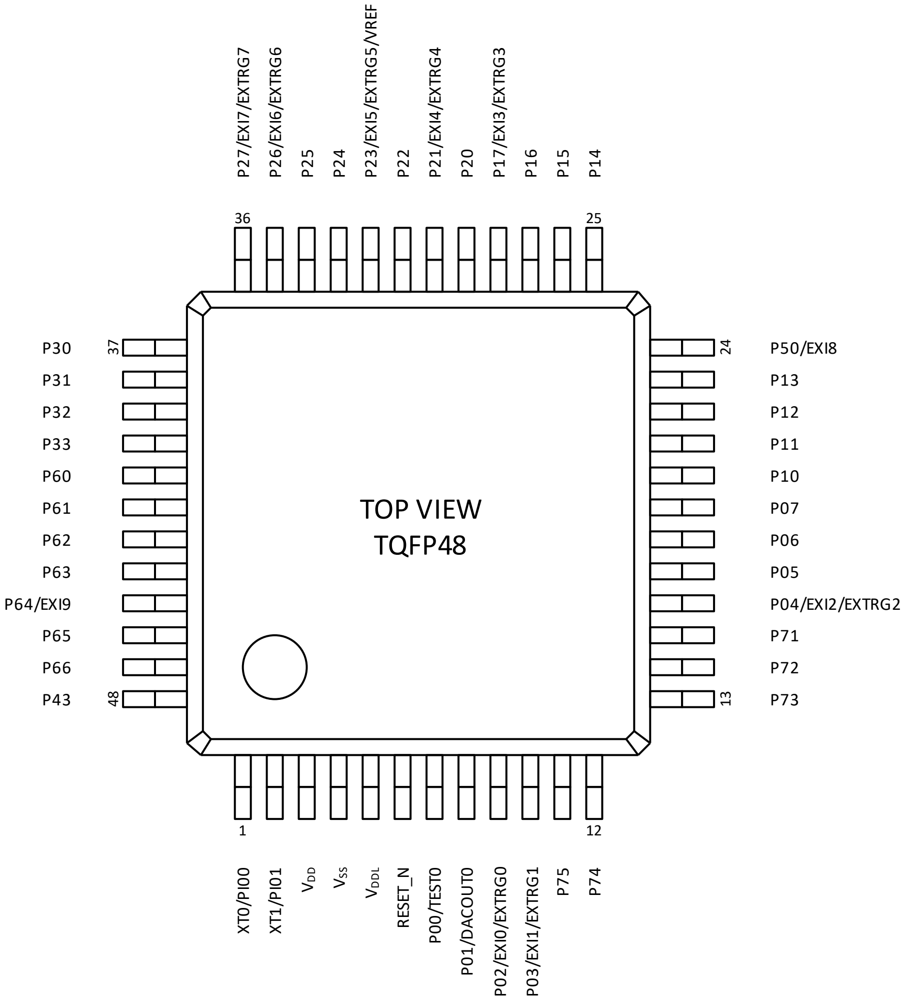


Figure 3 Pin Layout of 48pin TQFP Package

Pin Layout of 52pin TQFP Package

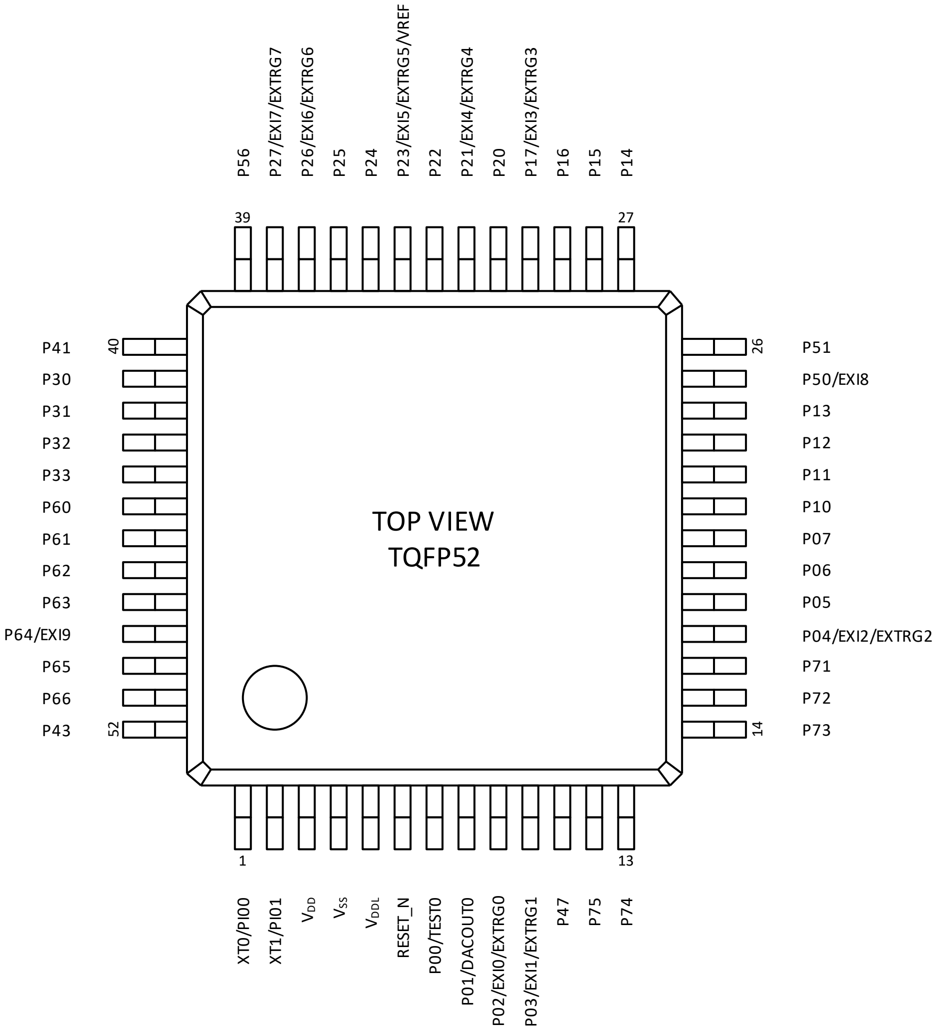


Figure 4 Pin Layout of 52pin TQFP Package

Pin Layout of 64pin TQFP/QFP Package

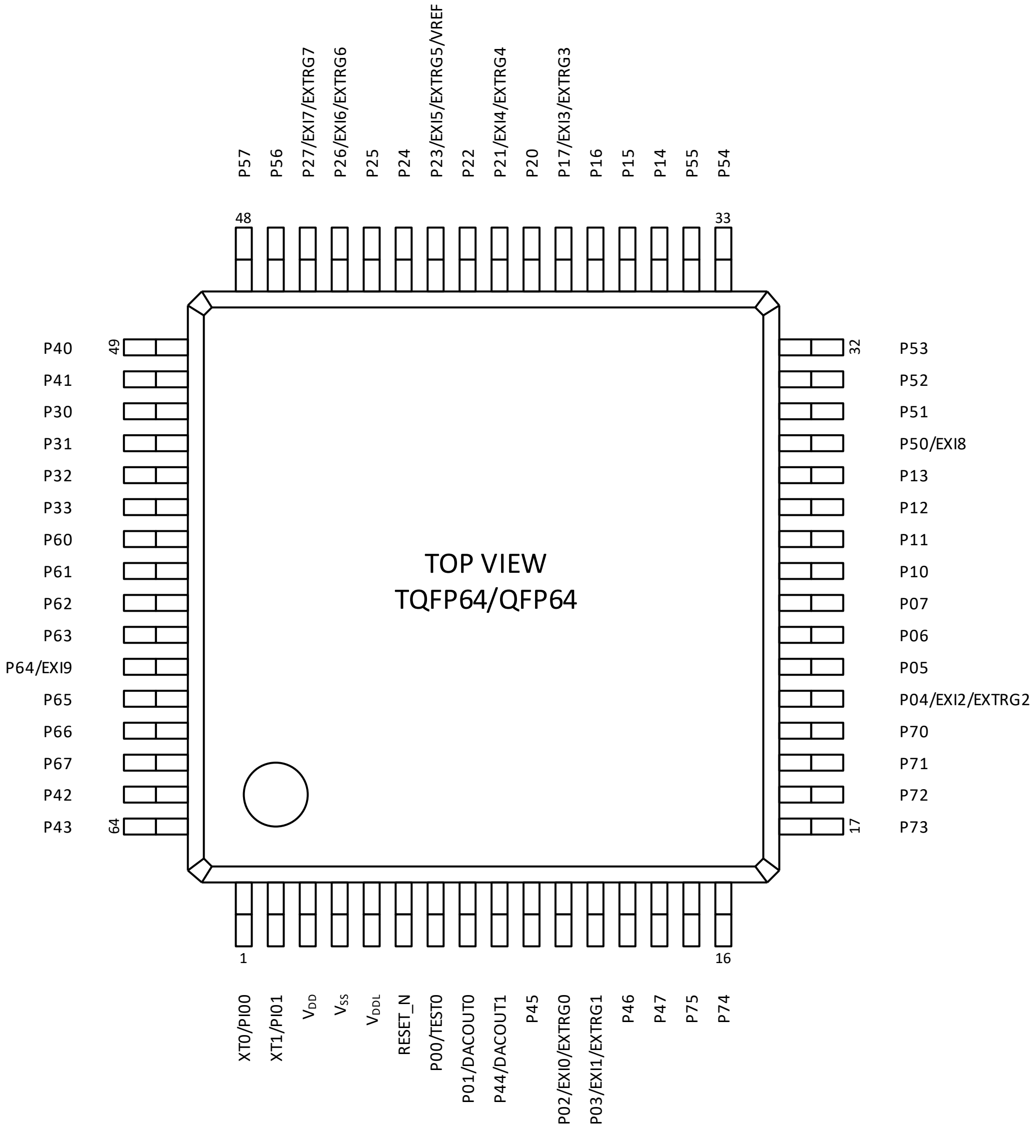


Figure 5 Pin Layout of 64pin TQFP/QFP Package

Pin Layout of 80pin QFP Package

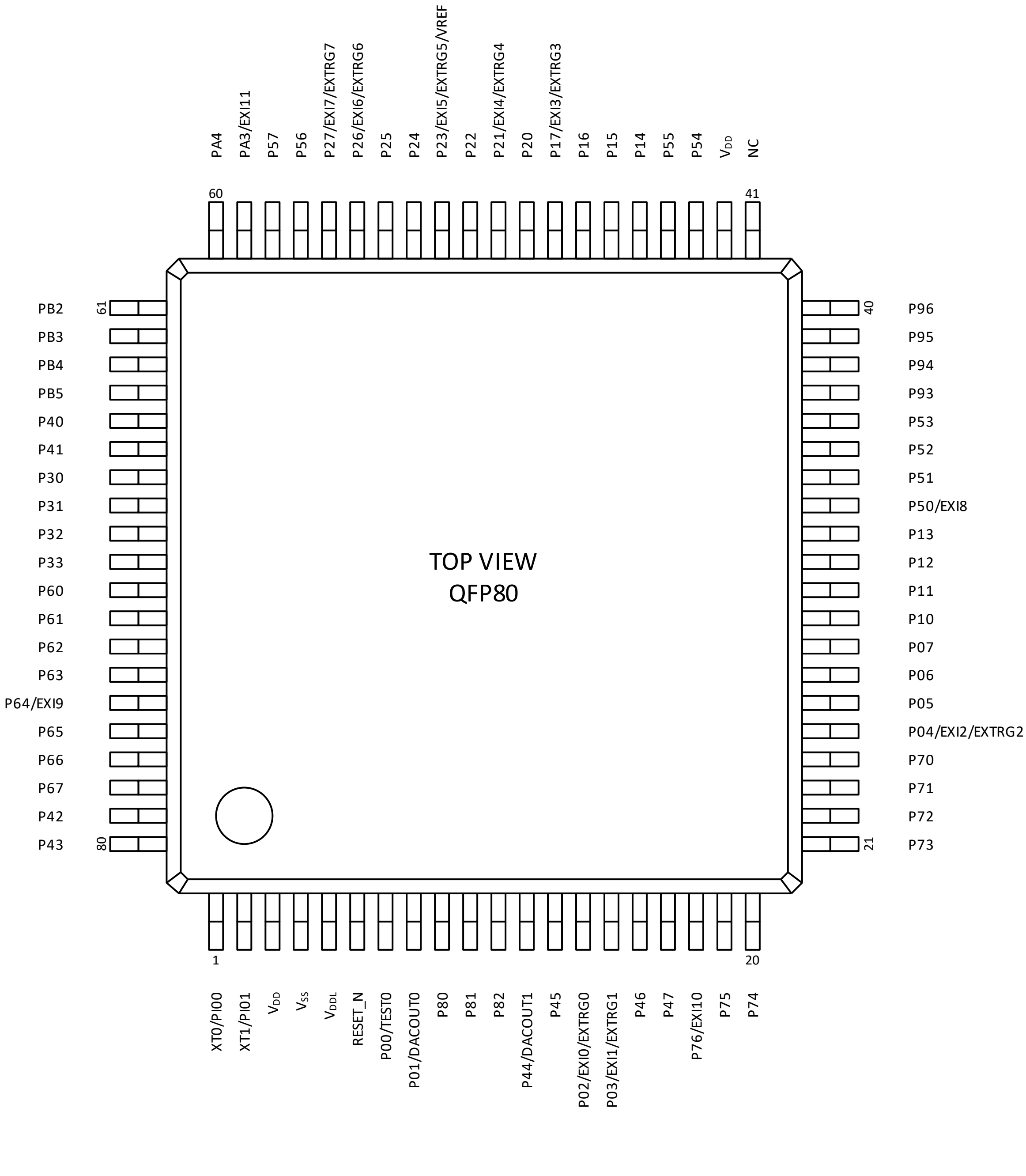


Figure 6 Pin Layout of 80pin QFP Package

Pin Layout of 100pin TQFP Package

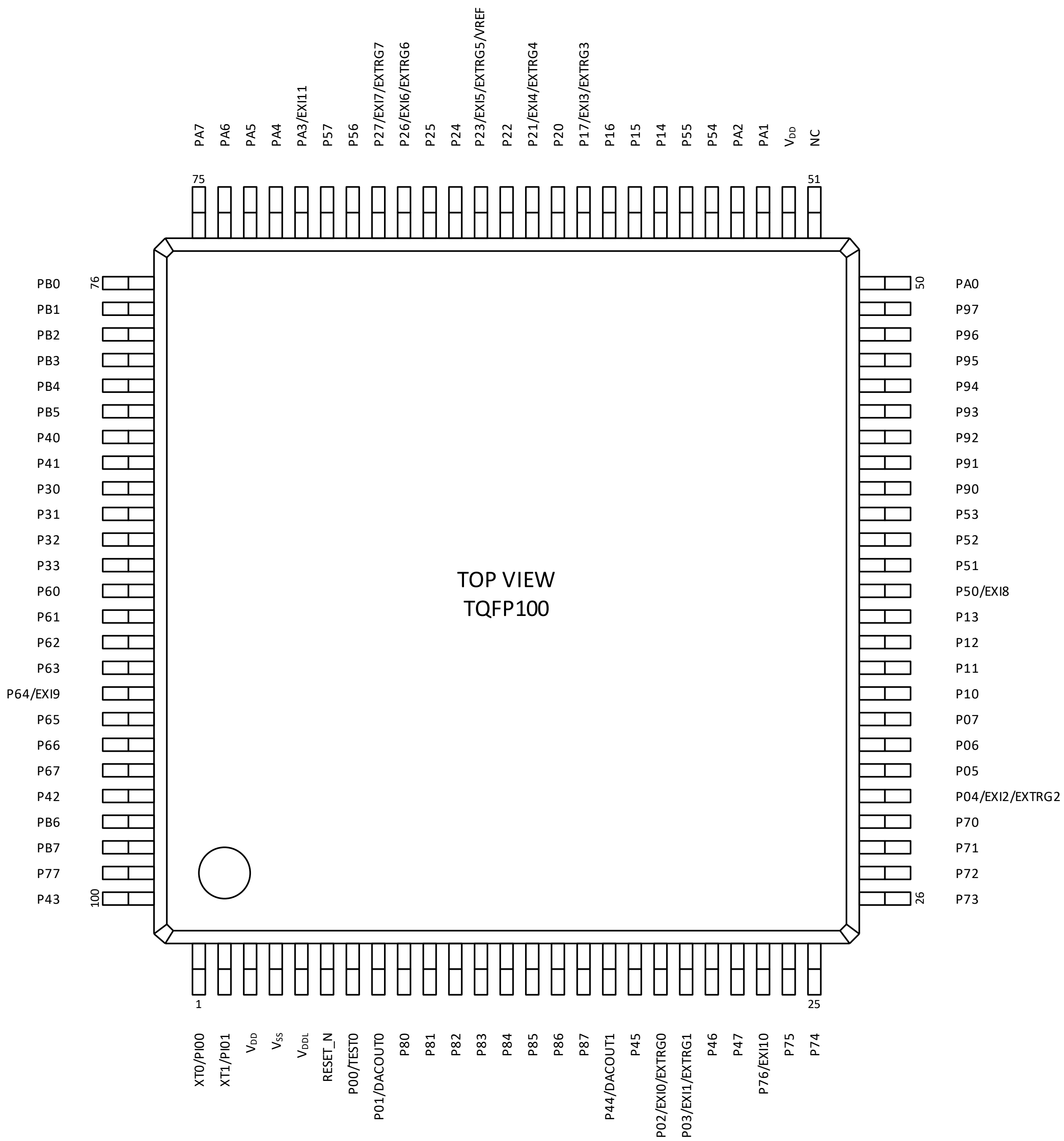


Figure 7 Pin Layout of 100pin TQFP Package

Pin Layout of 100pin QFP Package

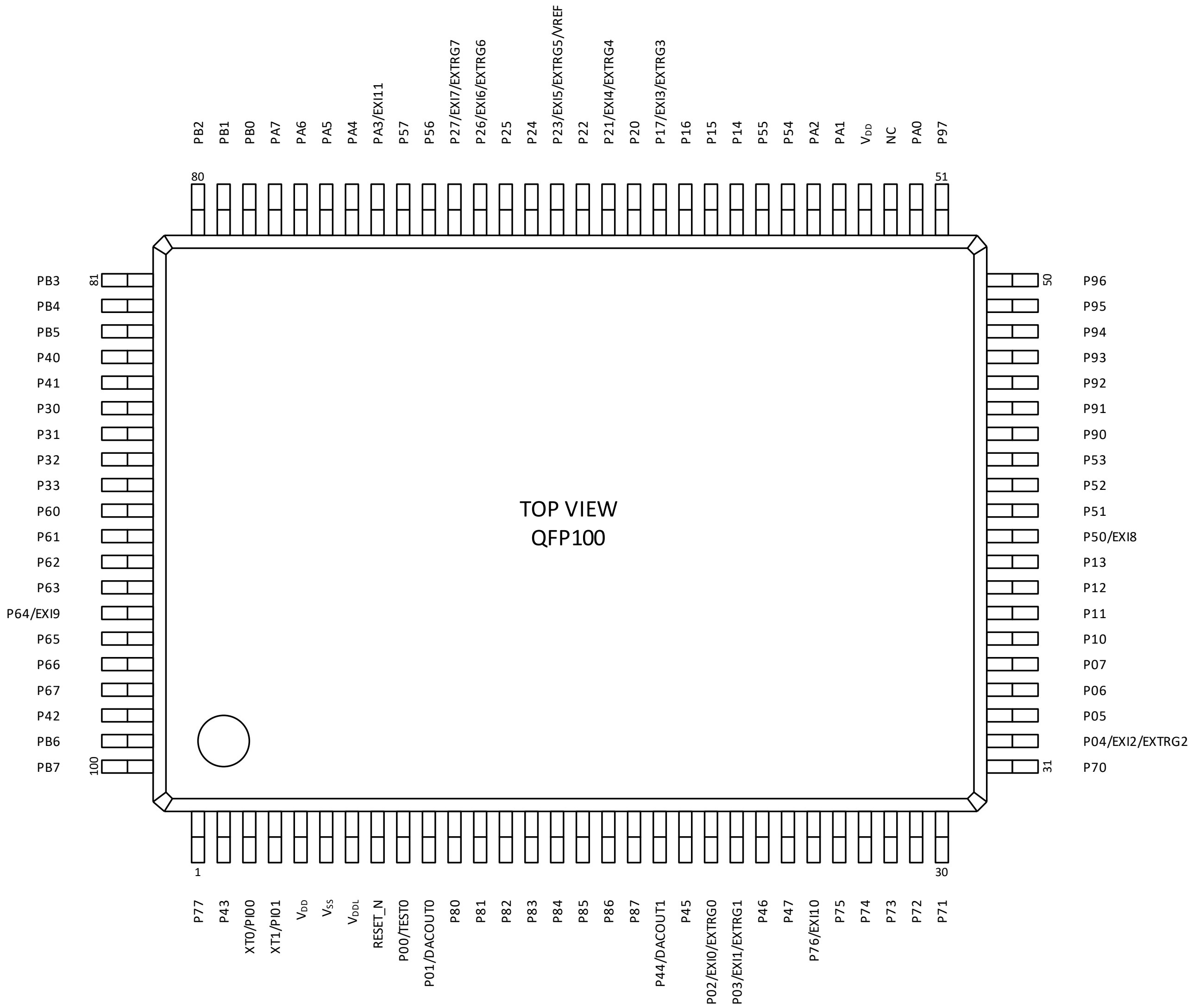


Figure 8 Pin Layout of 100pin QFP Package

PIN LIST

Table 3 Pin List (1/3)

Pin No.						Pin name (Primary func.)	Primary func. Others	2^{nd} func. SIU	3^{rd} func. SIU	4^{th} func. I2C	5^{th} func. Timer	6^{th} func. Others	7^{th} func. Others	8^{th} func. ADC
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100									
3	3	3	3	3	5	V_{DD}	-	-	-	-	-	-	-	-
-	-	-	42	52	54	V_{DD}	-	-	-	-	-	-	-	-
4	4	4	4	4	6	V_{SS}	-	-	-	-	-	-	-	-
-	-	-	41	51	53	NC	-	-	-	-	-	-	-	-
5	5	5	5	5	7	V_{DDL}	-	-	-	-	-	-	-	-
1	1	1	1	1	3	XT0	PI00	-	-	-	-	-	-	-
2	2	2	2	2	4	XT1	PI01	-	-	-	-	-	-	-
6	6	6	6	6	8	RESET_N	-	-	-	-	-	-	-	-
7	7	7	7	7	9	P00	TEST0	-	-	-	-	-	-	-
8	8	8	8	8	10	P01	DACOUT0	-	-	-	-	TBCOUT0	TBCOUT1	-
9	9	11	14	19	21	P02	EXI0 EXTRG0	SU0_RXD0 SU0_SIN	-	-	FTM0P	OUTLSCLK	CMP0M	-
10	10	12	15	20	22	P03	EXI1 EXTRG1	SU0_TXD0 SU0_SOUT	SU0_TXD1	I2CU0_SDA	FTM0N	OUTHSCLK	CMP0P	AIN11
16	17	21	25	30	32	P04	EXI2 EXTRG2	SU0_SCLK	-	I2CU0_SCL	TMH0OUT	-	-	-
17	18	22	26	31	33	P05	-	-	-	-	-	-	-	-
18	19	23	27	32	34	P06	-	-	-	I2CM0_SDA	-	-	-	-
19	20	24	28	33	35	P07	-	SU0_RXD1	SU0_RXD0	I2CM0_SCL	-	-	-	-
20	21	25	29	34	36	P10	-	SU0_TXD1	-	-	-	-	-	-
21	22	26	30	35	37	P11	-	SU0_SCLK	-	-	-	-	-	-
22	23	27	31	36	38	P12	-	SU0_RXD0 SU0_SIN	-	-	TMH4OUT	-	-	-
23	24	28	32	37	39	P13	-	SU0_TXD0 SU0_SOUT	SU0_TXD1	-	TMH1OUT	-	TMH3OUT	-
25	27	35	45	57	59	P14	-	-	-	-	-	-	-	-
26	28	36	46	58	60	P15	-	-	-	I2CU0_SDA		-	-	-
27	29	37	47	59	61	P16	-	SU1_SCLK	-	I2CU0_SCL	TMH5OUT	-	-	-
28	30	38	48	60	62	P17	EXI3 EXTRG3	SU0_RXD1	SU0_RXD0	-	FTM1P	TBCOUT0	BZ0P	AIN0
29	31	39	49	61	63	P20	-	SU0_TXD1	-	-	FTM1N	TBCOUT1	BZ0N	AIN1
30	32	40	50	62	64	P21	EXI4 EXTRG4	SU1_RXD0 SU1_SIN	-	-	FTM2P	OUTLSCLK	-	AIN2
31	33	41	51	63	65	P22	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	I2CM0_SDA	FTM2N	OUTHSCLK	-	AIN3
32	34	42	52	64	66	P23	EXI5 EXTRG5 V_{REF}	SU1_SCLK	-	I2CM0_SCL	TMH2OUT	-	-	V_{REFO}
33	35	43	53	65	67	P24	-	SU1_RXD0 SU1_SIN	-	-	-	-	-	AIN4
34	36	44	54	66	68	P25	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	-	-	-	-	AIN5
35	37	45	55	67	69	P26	EXI6 EXTRG6	SU1_RXD1	SU1_RXD0	I2CU0_SDA	FTM3P	TBCOUT0	BZ0P	AIN6
36	38	46	56	68	70	P27	EXI7 EXTRG7	SU1_TXD1	-	I2CU0_SCL	FTM3N	TBCOUT1	BZ0N	AIN7

Table 3 Pin List (2/3)

Pin No.						Pin name (Primary func)	Primary func. Others *1	2nd func. SIU *1	3rd func. SIU *1	4th func. I2C	5th func. Timer *1	6th func. Others	7th func. Others	8th func. ADC *1
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100									
37	41	51	67	84	86	P30	-	-	-	-	-	-	-	-
38	42	52	68	85	87	P31	-	-	-	-	-	TBCOUT0	TBCOUT1	-
39	43	53	69	86	88	P32	-	SU1_RXD1	SU1_RXD0	-	-	-	-	-
40	44	54	70	87	89	P33	-	SU1_TXD1	-	-	TMH3OUT	-	-	-
-	-	49	65	82	84	P40	-	SU5_TXD1	-	-	-	-	-	-
-	40	50	66	83	85	P41	-	-	-	-	-	-	-	-
-	-	63	79	96	98	P42	-	SU3_TXD1	-	-	-	-	-	-
48	52	64	80	100	2	P43	-	-	-	-	-	TBCOUT0	TBCOUT1	AIN10
-	-	9	12	17	19	P44	DACOUT1	SU4_RXD1	SU4_RXD0	-	-	-	-	-
-	-	10	13	18	20	P45	-	SU4_TXD1		-	-	-	-	-
-	-	13	16	21	23	P46	-	-	-	-	-	-	-	-
-	11	14	17	22	24	P47	-	-	-	-	-	-	-	-
24	25	29	33	38	40	P50	EXI8	-	-	-	-	-	-	-
-	26	30	34	39	41	P51	-	-	-	-	-	-	-	-
-	-	31	35	40	42	P52	-	SU4_RXD1	SU4_RXD0	-	-	-	-	-
-	-	32	36	41	43	P53	-	SU4_TXD1		-	-	-	-	-
-	-	33	43	55	57	P54	-	SU2_RXD1	SU2_RXD0	-	TMH7OUT	-	-	-
-	-	34	44	56	58	P55	-	SU2_TXD1	-	-	-	-	-	-
-	39	47	57	69	71	P56	-	SU2_RXD0 SU2_SIN	-	-	-	-	-	AIN12
-	-	48	58	70	72	P57	-	SU2_TXD0 SU2_SOUT	SU2_TXD1	-	-	-	-	AIN13
41	45	55	71	88	90	P60	-	-	-	I2CM1_SCL	-	-	-	-
42	46	56	72	89	91	P61	-	-	-	I2CM1_SDA	-	-	-	-
43	47	57	73	90	92	P62	-	-	-	-	FTM4N	-	CMP1P	-
44	48	58	74	91	93	P63	-	-	-	-	FTM4P	-	CMP1M	-
45	49	59	75	92	94	P64	EXI9	SU3_RXD0 SU3_SIN	-	-	FTM5P	-	-	-
46	50	60	76	93	95	P65	-	SU3_TXD0 SU3_SOUT	SU3_TXD1	-	FTM5N	-	-	AIN8
47	51	61	77	94	96	P66	-	SU3_SCLK	-	-	-	-	-	AIN9
-	-	62	78	95	97	P67	-	SU3_RXD1	SU3_RXD0	-	-	-	-	-
-	-	20	24	29	31	P70	-	-	-	-	TMH6OUT	-	-	-
15	16	19	23	28	30	P71	-	-	-	-	-	-	-	-
14	15	18	22	27	29	P72	-	-	-	-	-	-	-	-
13	14	17	21	26	28	P73	-	-	-	-	-	-	-	-
12	13	16	20	25	27	P74	-	-	-	-	-	-	-	-
11	12	15	19	24	26	P75	-	-	-	-	-	-	-	-
-	-	-	18	23	25	P76	EXI10	-	-	-	-	-	-	-
-	-	-	-	99	1	P77	-	-	-	-	-	-	-	-
-	-	-	9	9	11	P80	-	SU4_RXD0 SU4_SIN	-	-	-	-	-	-
-	-	-	10	10	12	P81	-	SU4_TXD0 SU4_SOUT	SU4_TXD1	-	-	-	-	-
-	-	-	11	11	13	P82	-	SU4_SCLK	-	-	-	-	-	-
-	-	-	-	12	14	P83	-	-	-	-	-	-	-	-
-	-	-	-	13	15	P84	-	-	-	-	-	-	-	-
-	-	-	-	14	16	P85	-	-	-	-	-	-	-	-
-	-	-	-	15	17	P86	-	-	-	-	-	-	-	-
-	-	-	-	16	18	P87	-	-	-	-	-	-	-	-

*1: The pins of name with DACOUT1, SU2, SU3, SU4, SU5, TMH6, TMH7, AIN12 or AIN13 are not assigned to products of 48/52/64 PIN-packages.

Table 3 Pin List (3/3)

Pin No. 48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100	Pin name (Primary func)	Primary func. Others	2nd func. SIU	3rd func. SIU	4th func. I2C	5th func. Timers	6th func. Others	7th func. Others	8th func. ADC
-	-	-	-	42	44	P90	-	-	-	-	-	-	-	-
-	-	-	-	43	45	P91	-	-	-	-	-	-	-	-
-	-	-	-	44	46	P92	-	-	-	-	-	-	-	-
-	-	-	37	45	47	P93	-	SU4_RXD0 SU4_SIN	-	-	FTM6P	-	-	-
-	-	-	38	46	48	P94	-	SU4_TXD0 SU4_SOUT	SU4_TXD1	-	FTM6N	-	-	-
-	-	-	39	47	49	P95	-	SU4_SCLK	-	-	-	-	-	-
-	-	-	40	48	50	P96	-	-	-	-	-	-	-	-
-	-	-	-	49	51	P97	-	-	-	-	-	-	-	-
-	-	-	-	50	52	PA0	-	-	-	-	-	-	-	-
-	-	-	-	53	55	PA1	-	-	-	-	-	-	-	-
-	-	-	-	54	56	PA2	-	-	-	-	-	-	-	-
-	-	-	59	71	73	PA3	EXI11	SU2_SCLK	-	-	FTM7P	-	-	AIN14
-	-	-	60	72	74	PA4	-	-	-	-	FTM7N	-	-	AIN15
-	-	-	-	73	75	PA5	-	-	-	-	-	-	-	-
-	-	-	-	74	76	PA6	-	-	-	-	-	-	-	-
-	-	-	-	75	77	PA7	-	-	-	-	-	-	-	-
-	-	-	-	76	78	PB0	-	-	-	-	-	-	-	-
-	-	-	-	77	79	PB1	-	-	-	-	-	-	-	-
-	-	-	61	78	80	PB2	-	SU5_RXD0 SU5_SIN	-	-	-	-	-	-
-	-	-	62	79	81	PB3	-	SU5_TXD0 SU5_SOUT	SU5_TXD1	-	-	-	-	-
-	-	-	63	80	82	PB4	-	SU5_SCLK	-	-	-	-	-	-
-	-	-	64	81	83	PB5	-	SU5_RXD1	SU5_RXD0	-	-	-	-	-
-	-	-	-	97	99	PB6	-	-	-	-	-	-	-	-
-	-	-	-	98	100	PB7	-	-	-	-	-	-	-	-

PIN DESCRIPTION

Table 4 Pin Description (1/5)

Function	Signal name	Pin name	I/O	Description	Logic
Power	―	V_{SS}	―	Negative power supply pin (-)	―
	―	V_{DD}	―	Positive power supply pin (+). Connect a capacitor C_V between this pin and V_{SS} to stabilize power supply.	―
	―	V_{DDL}	―	Power supply pin for internal logic (internal regulator's output). Connect a capacitor C_V（1μF） between this pin and $V_{SS.}$	―
Test	TEST0	P00	I/O	Input pin for testing. Also, used for on-chip debug interface or ISP function. P00 is initialized as pull-up input mode by the system reset (not high-impedance mode).	―
Un used	NC	NC	―	Recommended to connect to $V_{SS.}$	―
System	V_{REFO}	P23	―	Reference voltage output. An internal reference voltage in the SA type A/D converter block can be externally used for a reference. The pin is shared with the SA type A/D converter external reference voltage input.	―
	RESET_N	RESET_N	I	Input for reset. Asserting "L" level to this pin enters the MCU into system reset mode and internal circuits are initialized, then releasing it to "H" level make CPU start running the program. Used for on-chip debug interface or ISP function. Internal pull-up resistor is not installed.	Negative
	XT0	XT0	I	Low speed crystal oscillation pins Connect 32.768kHz crystal resonator and have capacitors between the pin and $V_{SS.}$	―
	XT1	XT1	O		―
	OUTLSCLK	P02 P21	O	Low-speed clock output.	―
	OUTHSCLK	P03 P22	O	High-speed clock output.	―
General input port (GPI)	PI00, PI01	XT0, XT1	I	General Input port Not available to use as general inputs when using the crystal resonator.	Positive
General port (GPIO)	P00	P00	I/O	General I/O port - High-impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output P00 is only initialized as pulled-up input and other ports are initialized as high-impedance. Not available to use as I/O pin when using for on-chip debug interface or ISP function.	Positive
	P01 – P07	P01 – P07	I/O	General I/O port - High-impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P10 – P17	P10 – P17			
	P20 – P27	P20 – P27			
	P30 – P33	P30 – P33			
	P40 – P47	P40 – P47			
	P50 – P57	P50 – P57			
	P60 – P67	P60 – P67			
	P70 – P77	P70 – P77			
	P80 – P87	P80 – P87			
	P90 – P97	P90 – P97			
	PA0 – PA7	PA0 – PA7			
	PB0 – PB7	PB0 – PB7			

Table 4 Pin Description (2/5)

Function	Signal name	Pin name	I/O	Description	Logic
UART	SU0_TXD0	P03 P13	O	Serial communication unit0/UART0 data output pin.	Positive
	SU0_RXD0	P02 P07 P12 P17	I	Serial communication unit0/UART0 data input pin.	Positive
	SU0_TXD1	P03 P10 P13 P20	O	Serial communication unit0/UART1 data output pin.	Positive
	SU0_RXD1	P07 P17	I	Serial communication unit0/UART1 data input pin.	Positive
	SU1_TXD0	P22 P25	O	Serial communication unit1/UART0 data output pin	Positive
	SU1_RXD0	P21 P24 P26 P32	I	Serial communication unit1/UART0 data input pin.	Positive
	SU1_TXD1	P22 P25 P27 P33	O	Serial communication unit1/UART1 data output pin.	Positive
	SU1_RXD1	P26 P32	I	Serial communication unit1/UART1 data input pin.	Positive
	SU2_TXD0	P57	O	Serial communication unit2/UART0 data output pin.	Positive
	SU2_RXD0	P54 P56	I	Serial communication unit2/UART0 data input pin.	Positive
	SU2_TXD1	P55 P57	O	Serial communication unit2/UART1 data output pin.	Positive
	SU2_RXD1	P54	I	Serial communication unit2/UART1 data input pin.	Positive
	SU3_TXD0	P65	O	Serial communication unit3/UART0 data output pin.	Positive
	SU3_RXD0	P64 P67	I	Serial communication unit3/UART0 data input pin.	Positive
	SU3_TXD1	P42 P65	O	Serial communication unit3/UART1 data output pin.	Positive
	SU3_RXD1	P67	I	Serial communication unit3/UART1 data input pin.	Positive
	SU4_TXD0	P81 P94	O	Serial communication unit4/UART0 data output pin.	Positive
	SU4_RXD0	P44 P52 P80 P93	I	Serial communication unit4/UART0 data input pin.	Positive
	SU4_TXD1	P45 P53 P81 P94	O	Serial communication unit4/UART1 data output pin.	Positive
	SU4_RXD1	P44 P52	I	Serial communication unit4/UART1 data input pin.	Positive
	SU5_TXD0	PB3 PB2	O	Serial communication unit5/UART0 data output pin.	Positive
	SU5_RXD0	PB5	I	Serial communication unit5/UART0 data input pin.	Positive
	SU5_TXD1	P40 PB3	O	Serial communication unit5/UART1 data output pin.	Positive
	SU5_RXD1	PB5	I	Serial communication unit5/UART1 data input pin.	Positive

Table 4 Pin Description (3/5)

Function	Signal name	Pin name	I/O	Description	Logic
Synchronous Serial Port	SU0_SIN	P02	I	Serial communication unit0/Synchronous serial data input pin.	Positive
		P12			
	SU0_SCK	P04	I/O	Serial communication unit0/Synchronous serial clock I/O pin.	Positive
		P11			
	SU0_SOUT	P03	O	Serial communication unit0/Synchronous serial data output pin.	Positive
		P13			
	SU1_SIN	P21	I	Serial communication unit1/Synchronous serial data input pin.	Positive
		P24			
	SU1_SCK	P16	I/O	Serial communication unit1/Synchronous serial clock I/O pin.	Positive
		P23			
	SU1_SOUT	P22	O	Serial communication unit1/Synchronous serial data output pin.	Positive
		P25			
	SU2_SIN	P56	I	Serial communication unit2/Synchronous serial data input pin.	Positive
	SU2_SCLK	PA3	I/O	Serial communication unit2/Synchronous serial clock I/O pin.	Positive
	SU2_SOUT	P57	O	Serial communication unit2/Synchronous serial data output pin.	Positive
	SU3_SIN	P64	I	Serial communication unit3/Synchronous serial data input pin.	Positive
	SU3_SCLK	P66	I/O	Serial communication unit3/Synchronous serial clock I/O pin.	Positive
	SU3_SOUT	P65	O	Serial communication unit3/Synchronous serial data output pin.	Positive
	SU4_SIN	P80	I	Serial communication unit4/Synchronous serial data input pin.	Positive
		P93			
	SU4_SCLK	P82	I/O	Serial communication unit4/Synchronous serial clock I/O pin.	Positive
		P95			
	SU4_SOUT	P81	O	Serial communication unit4/Synchronous serial data output pin.	Positive
		P94			
	SU5_SIN	PB2	I	Serial communication unit5/Synchronous serial data input pin.	Positive
	SU5_SCLK	PB4	I/O	Serial communication unit5/Synchronous serial clock I/O pin.	Positive
	SU5_SOUT	PB3	O	Serial communication unit5/Synchronous serial data output pin.	Positive
I^2C Bus	I2CU0_SDA	P03	I/O	I^2C Unit0 (Master and Salve) Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P15			
		P26			
	I2CU0_SCL	P04	I/O	I^2C Unit0 (Master and Salve) Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P16			
		P27			
	I2CM0_SDA	P06	I/O	I^2C Master0 Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P22			
	I2CM0_SCL	P07	I/O	I^2C Master0 Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P23			
	I2CM1_SDA	P61	I/O	I^2C Master1 Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
	I2CM1_SCL	P60	I/O	I^2C Master1 Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive

Table 4 Pin Description (4/5)

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer (FTM)	FTM0P	P02	O	Functional Timer0 output.	Positive
	FTM0N	P03	O	Functional Timer0 output.	Negative
	FTM1P	P17	O	Functional Timer1 output.	Positive
	FTM1N	P20	O	Functional Timer1 output.	Negative
	FTM2P	P21	O	Functional Timer2 output.	Positive
	FTM2N	P22	O	Functional Timer2 output.	Negative
	FTM3P	P26	O	Functional Timer3 output.	Positive
	FTM3N	P27	O	Functional Timer3 output.	Negative
	FTM4P	P63	O	Functional Timer4 output.	Positive
	FTM4N	P62	O	Functional Timer4 output.	Negative
	FTM5P	P64	O	Functional Timer5 output.	Positive
	FTM5N	P65	O	Functional Timer5 output.	Negative
	FTM6P	P93	O	Functional Timer6 output.	Positive
	FTM6N	P94	O	Functional Timer6 output.	Negative
	FTM7P	PA3	O	Functional Timer7 output.	Positive
	FTM7N	PA4	O	Functional Timer7 output.	Negative
	EXTRG0	P02	I	Functional Timer event trigger input pin.	—
	EXTRG1	P03	I	Functional Timer event trigger input pin.	—
	EXTRG2	P04	I	Functional Timer event trigger input pin.	—
	EXTRG3	P17	I	Functional Timer event trigger input pin.	—
	EXTRG4	P21	I	Functional Timer event trigger input pin.	—
	EXTRG5	P23	I	Functional Timer event trigger input pin.	—
	EXTRG6	P26	I	Functional Timer event trigger input pin.	—
	EXTRG7	P27	I	Functional Timer event trigger input pin.	—
16-bit Timer	TMH0OUT	P04	O	16bit General Timer0 output pin	Positive
	TMH1OUT	P13	O	16bit General Timer1 output pin	Positive
	TMH2OUT	P23	O	16bit General Timer2 output pin	Positive
	TMH3OUT	P13 P33	O	16bit General Timer3 output pin	Positive
	TMH4OUT	P12	O	16bit General Timer4 output pin	Positive
	TMH5OUT	P16	O	16bit General Timer5 output pin	Positive
	TMH6OUT	P70	O	16bit General Timer6 output pin	Positive
	TMH7OUT	P54	O	16bit General Timer7 output pin	Positive
	EXTRG0	P02	I	16bit General Timer event trigger input pin.	—
	EXTRG1	P03	I	16bit General Timer event trigger input pin.	—
Low-Speed Time Base Counter (LTBC)	TBCOUT0	P01 P17 P26 P31 P43	O	The virtual frequency adjustment signal or Low-speed Time Base Counter 1Hz/2Hz output pin	Positive
	TBCOUT1	P01 P20 P27 P31 P43	O	Low-speed Time Base Counter 1Hz/2Hz output pin	Positive
Buzzer	BZ0P	P17 P26	O	Buzzer output (positive phase)	Positive
	BZ0N	P20 P27	O	Buzzer output (negative phase)	Negative

Table 4 Pin Description (5/5)

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	GPIO maskable external interrupt pin	—
	EXI1	P03	I	GPIO maskable external interrupt pin	—
	EXI2	P04	I	GPIO maskable external interrupt pin	—
	EXI3	P17	I	GPIO maskable external interrupt pin	—
	EXI4	P21	I	GPIO maskable external interrupt pin	—
	EXI5	P23	I	GPIO maskable external interrupt pin	—
	EXI6	P26	I	GPIO maskable external interrupt pin	—
	EXI7	P27	I	GPIO maskable external interrupt pin	—
	EXI8	P50	I	GPIO maskable external interrupt pin	—
	EXI9	P64	I	GPIO maskable external interrupt pin	—
	EXI10	P76	I	GPIO maskable external interrupt pin	—
	EXI11	PA3	I	GPIO maskable external interrupt pin	—
Successive approximation type A/D converter	V_{REF}	P23	—	SA type A/D converter external reference voltage input. The voltage provided to the pin is used as the reference voltage for the A/D conversion.	—
	AIN0	P17	I	SA type A/D converter channel 0 input pin	—
	AIN1	P20	I	SA type A/D converter channel 1 input pin	—
	AIN2	P21	I	SA type A/D converter channel 2 input pin	—
	AIN3	P22	I	SA type A/D converter channel 3 input pin	—
	AIN4	P24	I	SA type A/D converter channel 4 input pin	—
	AIN5	P25	I	SA type A/D converter channel 5 input pin	—
	AIN6	P26	I	SA type A/D converter channel 6 input pin	—
	AIN7	P27	I	SA type A/D converter channel 7 input pin	—
	AIN8	P65	I	SA type A/D converter channel 8 input pin	—
	AIN9	P66	I	SA type A/D converter channel 9 input pin	—
	AIN10	P43	I	SA type A/D converter channel 10 input pin	—
	AIN11	P03	I	SA type A/D converter channel 11 input pin	—
	AIN12	P56	I	SA type A/D converter channel 12 input pin	—
	AIN13	P57	I	SA type A/D converter channel 13 input pin	—
	AIN14	PA3	I	SA type A/D converter channel 14 input pin	—
	AIN15	PA4	I	SA type A/D converter channel 15 input pin	—
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	—
	CMP0M	P02	I	Comparator input 0 (inverting input)	—
	CMP1P	P62	I	Comparator input 1 (noninverting input)	—
	CMP1M	P63	I	Comparator input 1 (inverting input)	—
D/A converter	DACOUT0	P01	O	D/A converter0 output pin	—
	DACOUT1	P44	O	D/A converter1 output pin	—

TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

Pin	Recommended pin termination
NC	Connect to V_{SS}.
RESET_N	Connect to V_{DD} through a resistor.
P00/TEST0	Open the pin with the internal initial condition of pulled-up input mode.
XT0/PI00, XT1/PI01	Open the pins with the internal initial condition of Hi-impedance mode.
P01 to P07	
P10 to P17	
P20 to P27	
P30 to P33	
P40 to P47	
P50 to P57	
P60 to P67	
P70 to P77	
P80 to P87	
P90 to P97	
PA0 to PA7	
PB0 to PB7	

Note:
For unused input ports or unused input/output ports, if an unstable middle level voltage is supplied to the corresponding pins which are configured as inputs without pull-up register or input/output mode, supply current may become excessively large. Therefore, it is recommended to configure those pins as either input mode with a pull-up resistor or output mode.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = +25°C		-0.3 to +2.0	V
Input voltage	V_{IN}	Ta = +25°C		-0.3 to V_{DD}+0.3*[1]	V
Output voltage1	V_{OUT1}	Ta = +25°C		-0.3 to V_{DD}+0.3*[1]	V
Output voltage2	V_{OUT2}	Ta = +25°C		-0.3 to +6.5	V
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*[2]	mA
			Total	-180*[2]	
"L" level output current	I_{OUTL}	Ta = +25°C	1pin	+40	mA
			Total	+180	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	—		-55 to +150	°C

*[1] 6.5V or lower
*[2] The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
[Note] Use the product within absolute maximum ratings. The absolute maximum ratings are conditions which may physically deteriorate the quality of product.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	-40 to +105	°C
Operating voltage 1	V_{DD}	—	1.6 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.6 to 5.5V	30k to 4M	Hz
		V_{DD} = 1.8 to 5.5V	30k to 25M	
V_{DDL} pin external capacitance	C_L	—	1.0 ±30%	μF

Operation Confirmed Crystal Unit (32.768kHz)

(V_{DD}=1.6 to 5.5V, V_{SS} =0V)

manufacturer	Part number	Temperature [°C]	Load capacitance CL[pF]	Oscillation mode			Oscillation circuit parameter *[1]*[2] (Reference data)	
				Low power	Standard	Tough	C_{DL} [pF]	C_{GL} [pF]
Kyocera	ST3215SB	-40 to +105	7	●	-	-	12	12
				-	●	●	13	13
			9	-	-	●	20	20
River-eletec	TFX-04	-40 to +105	5	●	-	-	8	8
				-	●	-	9	8
				-	-	●	10	10
Nihon Dempa Kogyo	NX3215SA	-40 to +85	9	●	●	●	15	15
SII	VT-200F	-40 to +85	6	●	-	-	9	9
			12.5	-	●	●	22	22
Daishinku	DST1610A	-40 to +85	6	-	●	●	10	10
	DT-26	-10 to +60	6	●	●	●	10	10
				-	●	●	22	22

* These are crystal units that operation with our reference board has been confirmed.
*[1] These include wiring and parasitic capacitance.
*[2] These are reference data. Please optimize them on user system.

Current Consumption 1

Product: ML62Q1530, ML62Q1531, ML62Q1532, ML62Q1533, ML62Q1534, ML62Q1540, ML62Q1541, ML62Q1542, ML62Q1543, ML62Q1544, ML62Q1550, ML62Q1551, ML62Q1552, ML62Q1553, ML62Q1554

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.*3	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.8	23	μA	1
			Ta = -40 to +105 °C	—		75		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	1.0	26	μA	
			Ta = -40 to +105 °C	—		80		
Supply current 2-1	IDD2-1	Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating*1). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	4.7	35	μA	
			Ta = -40 to +105 °C	—		85		
Supply current 2-2	IDD2-2	Low-speed Crystal Oscillating. *4 CPU is in HALT state (LTBC and WDT are operating*1). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	3.0	32	μA	
			Ta = -40 to +105 °C	—		85		
Supply current 3	IDD3	CPU: Running with low-speed RC32K oscillation clock*1*2 PLL oscillation is stopped.	Ta = -40 to +105 °C	—	17	105	μA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*1*2 PLL 16MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	3.3	4.5	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*1*2 PLL 24MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	4.7	6.0		

*1 LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all “1”
*2 CPU running in wait mode
*3 On the condition of V_{DD}=3.0V, Ta=+25°C
*4 When the noise filter is not used in the low power consumption mode

Current Consumption 2

Product: ML62Q1555, ML62Q1556, ML62Q1557, ML62Q1563, ML62Q1564, ML62Q1565, ML62Q1566, ML62Q1567, ML62Q1573, ML62Q1574, ML62Q1575, ML62Q1576, ML62Q1577

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.*[3]	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	1.0	55	μA	1
			Ta = -40 to +105 °C	—		110		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	1.3	60	μA	
			Ta = -40 to +105 °C	—		120		
Supply current 2-1	IDD2-1	Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating*[1]). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	5.5	76	μA	
			Ta = -40 to +105 °C	—		135		
Supply current 2-2	IDD2-2	Low-speed Crystal Oscillating.*[4] CPU is in HALT state (LTBC and WDT are operating*[1]). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	4.5	76	μA	
			Ta = -40 to +105 °C	—		135		
Supply current 3	IDD3	CPU: Running with low-speed RC32K oscillation clock*[1]*[2] PLL oscillation is stopped.	Ta = -40 to +105 °C	—	20	150	μA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*[1]*[2] PLL 16MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	5.0	6.2	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*[1]*[2] PLL 24MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	6.8	8.5		

*[1] LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all “1”
*[2] CPU running in wait mode
*[3] On the condition of V_{DD}=3.0V, Ta=+25°C
*[4] When the noise filter is not used in the low power consumption mode

Current Consumption 3

Product: ML62Q1558, ML62Q1559, ML62Q1568, ML62Q1569, ML62Q1578, ML62Q1579

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.*3	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	1.2	57	μA	1
			Ta = -40 to +105 °C	—		140		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	1.8	62	μA	
			Ta = -40 to +105 °C	—		150		
Supply current 2-1	IDD2-1	Low-speed RC32K Oscillating. CPU is in HALT state (LTBC and WDT are operating*1). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	6.0	78	μA	
			Ta = -40 to +105 °C	—		165		
Supply current 2-2	IDD2-2	Low-speed Crystal Oscillating.*4 CPU is in HALT state (LTBC and WDT are operating*1). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	4.5	78	μA	
			Ta = -40 to +105 °C	—		165		
Supply current 3	IDD3	CPU: Running with low-speed RC32K oscillation clock*1*2 PLL oscillation is stopped.	Ta = -40 to +105 °C	—	20	190	μA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*1*2 PLL 16MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	4.0	5.0	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*1*2 PLL 24MHz is oscillating. V_{DD}=1.8~5.5V	Ta = -40 to +105 °C	—	5.7	7.0		

*1 LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all “1”

*2 CPU running in wait mode

*3 On the condition of V_{DD}=3.0V, Ta=+25°C

*4 When the noise filter is not used in the low power consumption mode

Low speed Crystal Oscillation

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

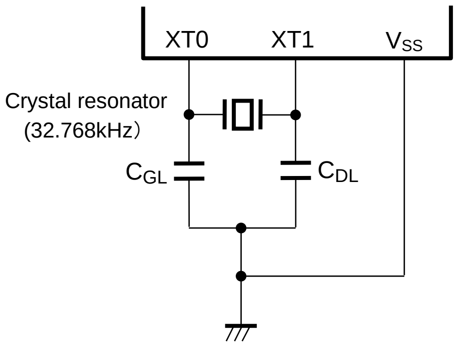
Parameter	Symbol	Condition	Range			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequency *1 *2	f_{XTL}	—	—	32.768	—	kHz
Crystal oscillation start time	T_{XTL}	—	—	—	2	s

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator and the external capacitance (C_{GL}/C_{DL}). As those parameters changes depending the crystal resonator, it requires evaluation on the actual PCB circuit for matching. Ask crystal resonator makers for matching and confirm the oscillation characteristics.

*2: The quality of oscillation characteristics might be lost, depending on material of PCB, condition of wiring capacitance or parasitic capacitance on the external circuits. Note for designing the external circuit.

- Make the wires on the external circuit as short as possible.
- Place the crystal resonator and oscillation circuit as close to the MCU as possible and make the wires between the external capacitance and crystal resonator as short as possible.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
  variation.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

Low speed Crystal Oscillation external circuit example



External Clock Input

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Range			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	—	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input pulse width	t_{EXCKW}	—	1/fEXCK x 0.4	—	1/fEXCK x 0.6	s

On-chip Oscillator

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency accuracy 1	f_{RCL1}	Ta= +25°C V_{DD} = 1.8 to 5.5V Without software adjustment *[1]	Typ. -1.0%	32.768	Typ. +1.0%	kHz	1
		Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V Without software adjustment *[1]	Typ. -2.5%	32.768	Typ. +2.5%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V Without software adjustment *[1]	Typ. -3.0%	32.768	Typ. +3.0%		
		V_{DD} = 1.6 to 1.8V Without software adjustment *[1]	Typ. -3.5%	32.768	Typ. -3.5%		
Low-speed RC oscillator frequency accuracy 2	f_{RCL2}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V With software adjustment *[1]	Typ. -1.0%	32.768	Typ. +1.0%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V With software adjustment *[1]	Typ. -1.5%	32.768	Typ. +1.5%		
PLL oscillation frequency accuracy 1	f_{PLL1}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V Without software adjustment *[1]	Typ. -2.5%	16/24	Typ. +2.5%	MHz	
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V Without software adjustment *[1]	Typ. -3.0%	16/24	Typ. +3.0%		
		V_{DD} = 1.6 to 1.8V Without software adjustment *[1]	Typ. -3.5%	16/24	Typ. +3.5%		
PLL oscillation frequency accuracy 2	f_{PLL2}	Ta= -40 to +85°C V_{DD} = 1.8 to 5.5V With software adjustment *[1]	Typ. -1.0%	16/24	Typ. +1.0%		
		Ta= -40 to +105°C V_{DD} = 1.8 to 5.5V With software adjustment *[1]	Typ. -1.5%	16/24	Typ. +1.5%		
PLL oscillation start time	T_{PLL}	V_{DD} = 1.6 to 5.5V	—	—	2	ms	
1kHz Low-speed RC oscillator (for WDT) frequency accuracy	f_{RC1K}	Ta= -40 to +105°C V_{DD} = 1.6 to 5.5V	0.5	1	2.5	kHz	

*[1] Adjust the frequency by using temperature sensor in ADC and a Specific Function Register (LRCADJ register)

Input / Output pin 1

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage1 "H"/"L" level (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7)	VOH1	IOH1=-10mA V_{DD}≥4.5V	V_{DD} -1.5	—	—	V	2
		IOH1=-1mA V_{DD}≥1.6V	V_{DD} -0.5	—	—		
	VOL1	IOL1=+10mA V_{DD}≥4.5V	—	—	1.5		
		IOL1=+1mA V_{DD}≥1.6V	—	—	0.5		
Output voltage2 "L" level (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7)	VOL2	When Nch open drain output mode is selected: IOL2=+15mA V_{DD}≥4.5V	—	—	0.7		
		When Nch open drain output mode is selected: IOL2=+8mA V_{DD}≥3.0V	—	—	0.5		
		When Nch open drain output mode is selected: IOL2=+3mA V_{DD}≥2.0V	—	—	0.4		
		When Nch open drain output mode is selected: IOL2=+2mA V_{DD}≥1.6V	—	—	0.4		

Input / Output pin 2

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V_{DD}≥4.5V	-10*3*5	—	—	mA	3
			V_{DD}≥1.6V	-1*3*5	—	—		
"H" level output total current *1*4	IOH3	Total of 'P00-P07, P10-P13, P44-P47, P50-P53, P70-P76, P80-P87, P90-P97, PA0' or 'P14-P17, P20-P27, P30-P33, P40-P43, P54-P57 P60-P67,P77, PA1-PA7, PB0-PB7' (duty≤50%)	V_{DD}≥4.5V	-90*5	—	—		
			V_{DD}≥1.6V	-20*5	—	—		
		All pin total (duty≤50%)	V_{DD}≥4.5V	-180*5	—	—		
			V_{DD}≥1.6V	-40*5	—	—		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V_{DD}≥4.5V	—	—	10*3		
			V_{DD}≥1.6V	—	—	1*3		
"L" level output current2 *6	IOL2	1pin (Nch open drain output mode)	V_{DD}≥4.5V	—	—	15*3		
			V_{DD}≥3.0V	—	—	8*3		
			V_{DD}≥2.0V	—	—	3*3		
			V_{DD}≥1.6V	—	—	2*3		
"L" level output total current *2*4	IOL3	Total of P00-P07, P10-P13, P44-P47, P50-P53, P70-P76, P80-P87, P90-P97, PA0' or 'P14~P17, P20-P27, P30-P33, P40-P43, P54-P57 P60-P67,P77, PA1-PA7, PB0-PB7' (Nch open drain output mode,duty≤50%)	V_{DD}≥4.5V	—	—	90		
			V_{DD}≥3.0V	—	—	40		
			V_{DD}≥2.0V	—	—	15		
			V_{DD}≥1.6V	—	—	10		
		All pin total (Nch open drain output mode,duty≤50%)	V_{DD}≥4.5V	—	—	180		
			V_{DD}≥1.6V	—	—	20		
Output leak (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7)	IOOH	VOH=V_{DD} (High impedance mode)		—	—	+1	μA	
	IOOL	VOL=V_{SS} (High impedance mode)		-1*5	—	—		

*[1] Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.
*[2] Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.
*[3] Do not beyond total current.
*[4] The total current is on the condition of Duty≤50%(same applies to IOH1).
When the duty>50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3=100mA and n=80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*[5] The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*[6] These values are satisfied with VOH1, VOL1 and VOL2.

Input / Output pin 3

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current1 (RESET_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-1*1	—	—		
Input current2 (P00/TEST0)	IIL2	VIL2=V_{SS} (pull-up mode)*2	-1500*1	-300*1	-20*1		
	V/IIL2	VIL2=V_{SS} (pull-up mode) *2	3.7	10	80	kΩ	
	IIH2Z	VIH2=V_{DD} (High impedance mode)	—	—	1	μA	
	IIL2Z	VIL2=V_{SS} (High impedance mode)	-1*1	—	—		
Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7)	IIL3	VIL3=V_{SS}(pull-up mode) *2	-250*1	-30*1	-2*1		
	V/IIL3	VIL3=V_{SS} (pull-up mode) *2	22	100	800	kΩ	
	IIH3Z	VIH3=V_{DD} (High impedance mode)	—	—	1	μA	
	IIL3Z	VIL3=V_{SS} (High impedance mode)	-1*1	—	—		
Input current4 (PI00-PI01)	IIH4	VIH4=V_{DD}	—	—	1		
	IIL4	VIL4=V_{SS}	-1*1	—	—		
Input voltage1 (RESET_N) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) (PI00-PI01)	VIH1	—	0.7 x V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3 x V_{DD}		
Input voltage2 (P00/TEST0)	VIH2	—	0.7 x V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.25 x V_{DD}		
Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P87) (P90-P97) (PA0-PA7) (PB0-PB7) (PI00-PI01)	CPIN	f = 10kHz Ta = +25°C	—	—	10	pF	—

*1 The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

*2 Measurement conditions: Typ. : V_{DD} = 3.0V, Max. : V_{DD} = 1.6V, Min. : V_{DD} = 5.5V

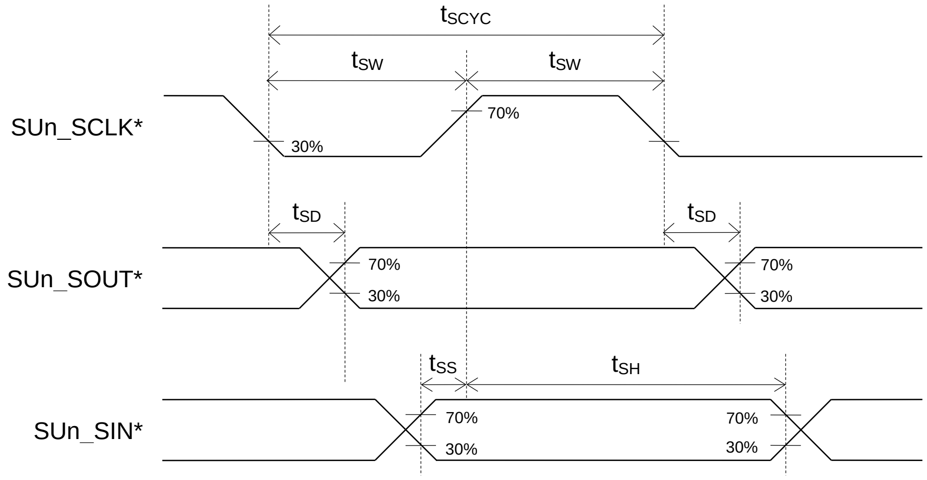
Synchronous Serial Port

Slave mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle	t_{SCYC}	—	1 *[2]	—	—	µs
SCK input pulse width	t_{SW}	—	0.5 *[3]	—	—	µs
SOUT output delay time	t_{SD}	V_{DD}=2.4 to 5.5V	—	—	100+ HSCLK*[1]×3	ns
		V_{DD}=1.8 to 5.5V	—	—	200+ HSCLK*[1]×3	ns
SIN input setup time	t_{SS}	—	HSCLK*[1] x1	—	—	ns
SIN input hold time	t_{SH}	—	80+ HSCLK*[1]×3	—	—	ns

*[1] Cycle of high speed clock
*[2] Need input cycles of HSLCK x8 or longer
*[3] Need input cycles of HSLCK x4 or longer



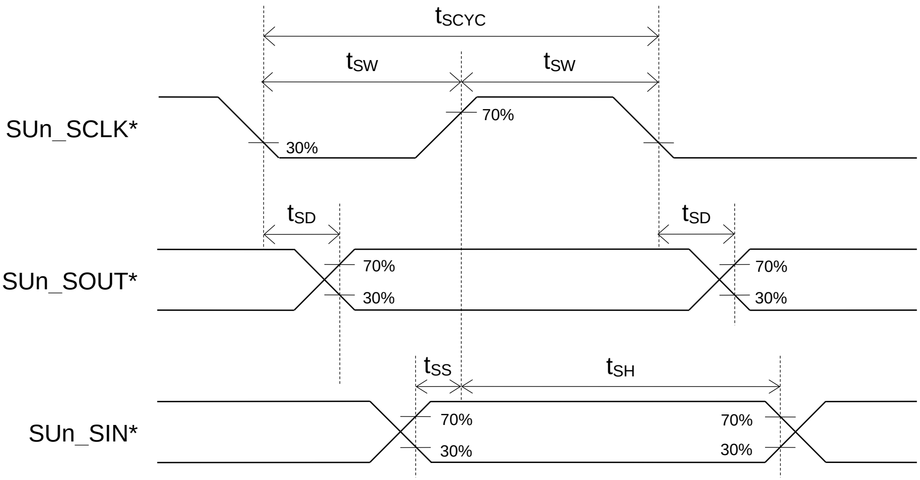
* 2nd to 8th function of port, n=0~5

Master mode

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK output cycle	t_{SCYC}	—	—	SCLK*[1]	—	ns
SCK output pulse width	t_{SW}	—	SCLK*[1] ×0.4	SCLK*[1] ×0.5	SCLK*[1] ×0.6	ns
SOUT output delay time	t_{SD}	V_{DD}=2.4 to 5.5V	—	—	100	ns
		V_{DD}=1.8 to 5.5V	—	—	160	ns
SIN input setup time	t_{SS}	V_{DD}=2.4 to 5.5V	120	—	—	ns
		V_{DD}=1.8 to 5.5V	180	—	—	ns
SIN input hold time	t_{SH}	V_{DD}=2.4 to 5.5V	80	—	—	ns
		V_{DD}=1.8 to 5.5V	100	—	—	ns

*[1] Clock cycle selected by bit12~8(SnCK4~0) of the serial port n mode register (SIOnMOD)
V_{DD}≥2.4V: min250ns , V_{DD}≥1.8V: min500ns



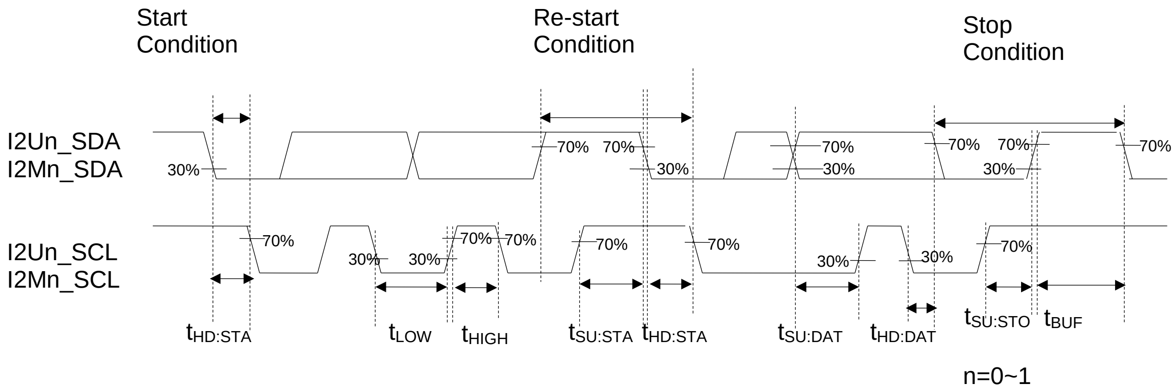
* 2nd to 8th function of port, n=0~5

Standard Mode 100kHz

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	μs
SCL "L" level time	t_{LOW}	—	4.7	—	—	μs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	μs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	μs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	μs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	μs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	μs
Bus-free time	t_{BUF}	—	4.7	—	—	μs

When using the I^2C as the master, configure the I^2C master n mode register(I2MnMOD) and I^2C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

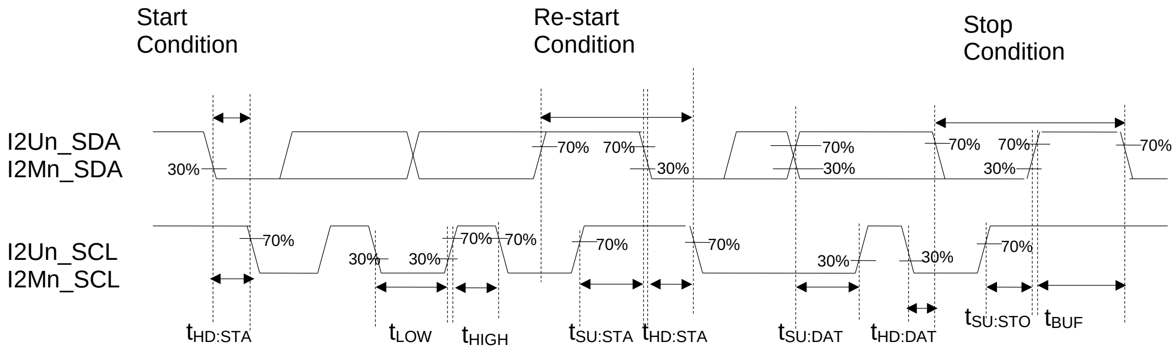


Fast Mode 400kHz

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	μs
SCL "L" level time	t_{LOW}	—	1.3	—	—	μs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	μs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	μs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	μs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	μs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	μs
Bus-free time	t_{BUF}	—	1.3	—	—	μs

When using the I^2C as the master, configure the I^2C master n mode register(I2MnMOD) and I^2C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



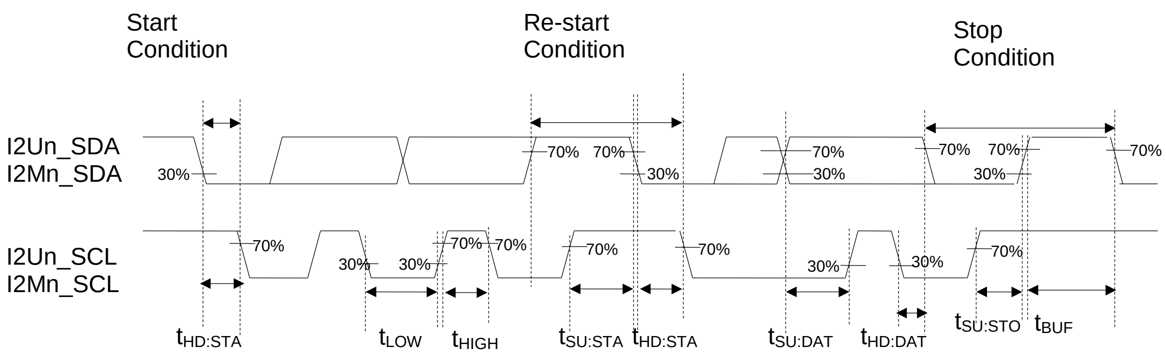
n=0~1

1Mbps Mode

(V_{DD}=2.7 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.26	—	—	µs
SCL "L" level time	t_{LOW}	—	0.5	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.26	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.26	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.26	—	—	µs
Bus-free time	t_{BUF}	—	0.5	—	—	µs

When using the I^2C as the master, configure the I^2C master n mode register(I2MnMOD) and I^2C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

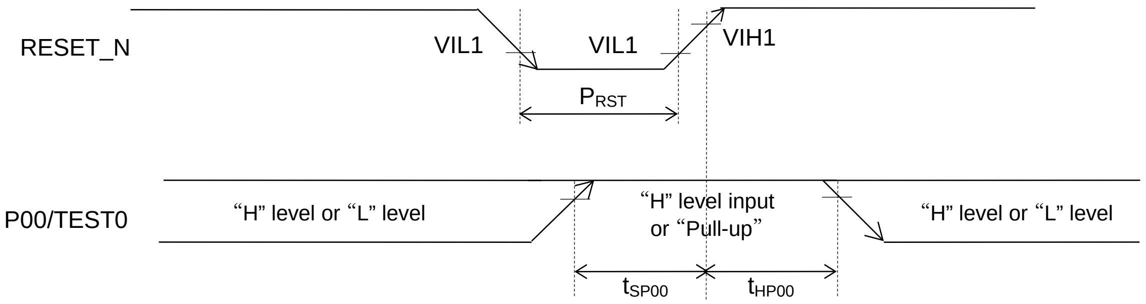


n=0~1

Reset

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width	P_{RST}	—	2	—	—	ms	1
P00 ”H” level setup time	t_{SP00}	—	1	—	—	ms	
P00 ”H” level hold time	t_{HP00}	—	1	—	—	ms	

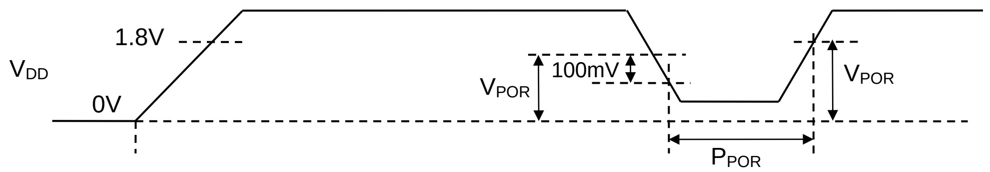


Power On Reset

(V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
POR detect voltage	V_{POR}	Power down(falling)	1.43	1.49	1.58	V	1
		Power up(rising)	1.47	1.57	1.80	V	
Power on rising slope	R_{POR}*[1]	—	—	—	60	V/ms	
POR response time	P_{POR}	*[2]	200	—	—	μs	

*[1]: Rise the V_{DD} to 1.8V or higher when powering on.
*[2]: This is the time from the V_{DD} gets 100mV lower than V_{POR} to the Power-On-Reset internally generates.
Make the power down falling slope 2V/ms or lower(i.e. slower).



[Note for in case of instantaneous power failure]

In case of instantaneous power failure and a pulse shorter than the response time of VLS or POR is asserted to V_{DD}, it is possible to make the MCU cannot get the reset and make erroneous operation. In that case, please have countermeasures such as preventing the voltage down using bypass capacitor or making reset pin reset.

VLS

(V_{DD}=1.6 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition VLS0LV *[1]		Min.	Typ.	Max.	Unit	Measuring circuit
VLS threshold voltage *[2]	V_{VLSR}	00H	Rising	3.86	4.06	4.26	V	1
	V_{VLSF}		Falling	3.84	4.00	4.16		
	V_{VLSR}	01H	Rising	3.57	3.76	3.95		
	V_{VLSF}		Falling	3.55	3.70	3.85		
	V_{VLSR}	02H	Rising	2.94	3.11	3.28		
	V_{VLSF}		Falling	2.92	3.05	3.18		
	V_{VLSR}	03H	Rising	2.85	3.01	3.17		
	V_{VLSF}		Falling	2.83	2.95	3.07		
	V_{VLSR}	04H	Rising	2.75	2.91	3.07		
	V_{VLSF}		Falling	2.73	2.85	2.97		
	V_{VLSR}	05H	Rising	2.66	2.81	2.96		
	V_{VLSF}		Falling	2.64	2.75	2.86		
	V_{VLSR}	06H	Rising	2.56	2.71	2.86		
	V_{VLSF}		Falling	2.54	2.65	2.76		
	V_{VLSR}	07H	Rising	2.46	2.61	2.76		
	V_{VLSF}		Falling	2.44	2.55	2.66		
	V_{VLSR}	08H	Rising	2.37	2.51	2.65		
	V_{VLSF}		Falling	2.35	2.45	2.55		
	V_{VLSR}	09H	Rising	1.98	2.11	2.24		
	V_{VLSF}		Falling	1.96	2.05	2.14		
	V_{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V_{VLSF}		Falling	1.87	1.95	2.03		
	V_{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V_{VLSF}		Falling	1.77	1.85	1.93		
VLS Current	I_{VLS}	—		—	50	—	nA	

*[1] Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).

*[2] The Data VSL0LV = 0CH~0FH is not available to use, if the data is specified it will the same spec as that 0BH is specified.

Analog Comparator

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Comparator same phase input voltage range	V_{CMR}	—	0.1	—	V_{DD} -1.5	V	1
Comparator0 input offset	V_{CMOF}	Ta=+25°C、V_{DD}=5.0V	—	5	—	mV	
Comparator Reference Voltage	V_{CMREF}	—	0.75	0.8	0.85	V	

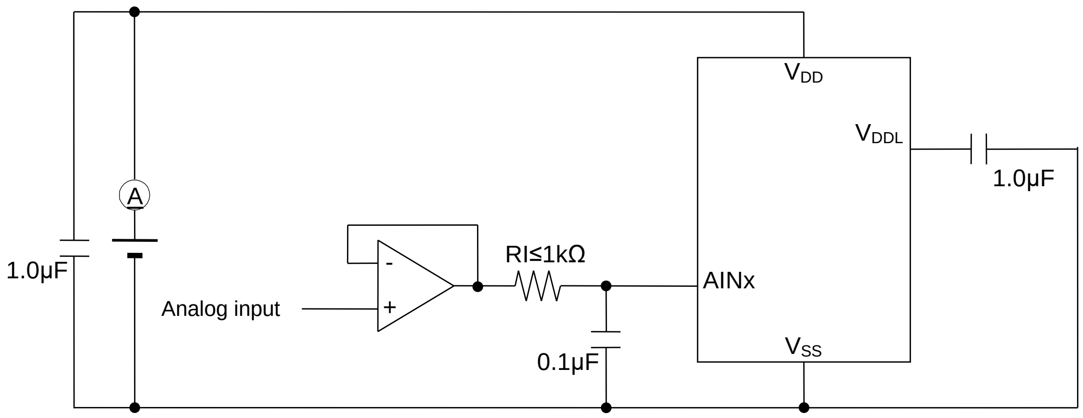
Successive Approximation Type A/D Converter

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{AD}	—	—	—	10	bit
Overall error	—	4.5V≤V_{REFP} *1≤5.5V	-3.5	1.2	3.5	LSB
Integral non-linearity error	INL_{AD}	2.7V≤V_{REFP} *1≤5.5V	-4	—	4	
		2.2V≤V_{REFP} *1<2.7V	-6	—	6	
		1.8V≤V_{REFP} *1<2.2V	-10	—	10	
		V_{REFP}=Internal reference voltage	-15	—	15	
Differential non-linearity error	DNL_{AD}	2.7V≤V_{REFP} *1≤5.5V	-3	—	3	
		2.2V≤V_{REFP} *1<2.7V	-5	—	5	
		1.8V≤V_{REFP} *1<2.2V	-9	—	9	
		V_{REFP}=Internal reference voltage	-14	—	14	
Zero-scale error	ZSE	RI≤1kΩ	-6	—	6	
Full-scale error	FSE	RI≤1kΩ	-6	—	6	
A/D reference voltage	V_{REF}	—	1.8	—	V_{DD}	V
Internal reference voltage	V_{REFI}	—	1.5	1.55	1.6	
Conversion time	t_{CONV}	4.5V≤V_{DD}≤5.5V	2.25	—	427	μs
		2.2V≤V_{DD}≤5.5V	4.5	—	427	
		1.8V≤V_{DD}≤5.5V	18	—	427	

*1 : V_{DD} or P23/V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter by setting bit5(VREFP1) and bit4(VREFP0) of Reference voltage control register(VREFCON).

The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1uF capacitor on the ADC input pin is recommended to reduce the noise.



D/A Converter

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{DA}	—	—	—	8	bit
Conversion cycle	tc	—	10	—	—	μs
Integral non-linearity error	INL_{DA}	RL=4MΩ	-2	—	2	LSB
Differential non-linearity error	DNL_{DA}	RL=4MΩ	-1	—	1	
Output impedance	Ro	DACEN bit of D/A converter enable register =1	3	6	9	kΩ

Reference Voltage Output

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REFO}	—	—	1.55	—	V
Output impedance	R_{VREFO}	—	—	—	500	kΩ

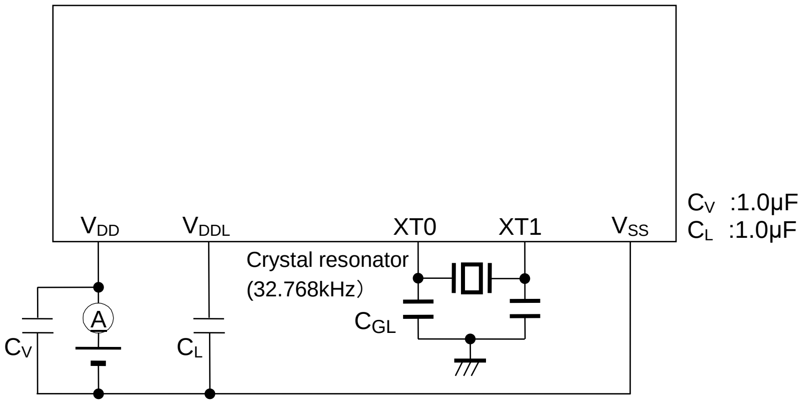
Flash Memory

(V_{SS}= 0V)

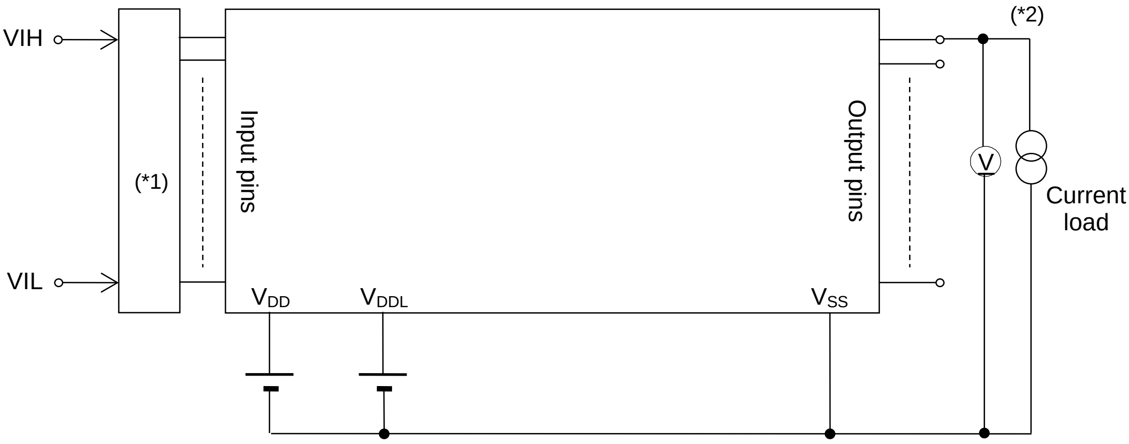
Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash		10000	times
	CEPP	Program Flash		100	
Erase unit	—	Block erase	Program Flash	16K	B
			Data Flash	all area	
	—	Sector erase	Program Flash	1K	B
			Data Flash	128	
Erase time (Max.)	—	Block erase / Sector erase		50	ms
Write unit	—	Program Flash		4	B
		Data Flash		1	
Write time (Max.)	—	Program Flash		80	μs
	—	Data Flash		40	
Data retention period	YDR	—		15	years

Measuring circuit

Measuring circuit 1

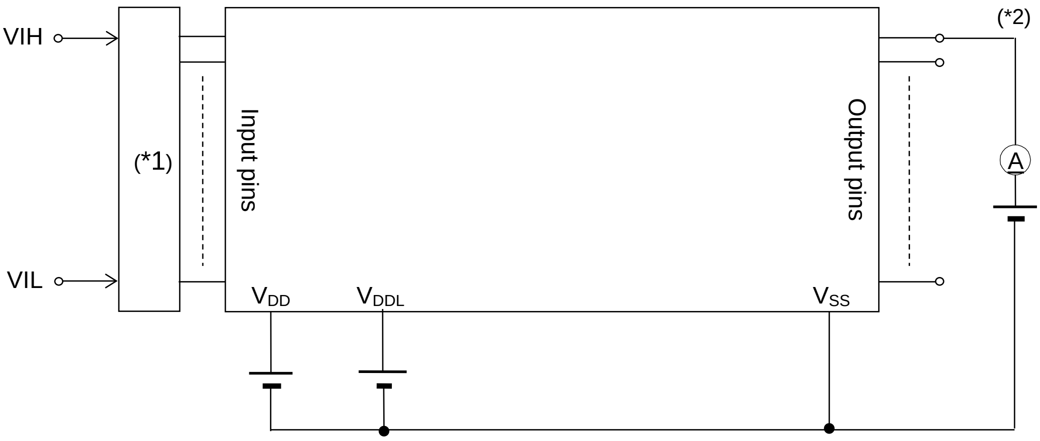


Measuring circuit 2



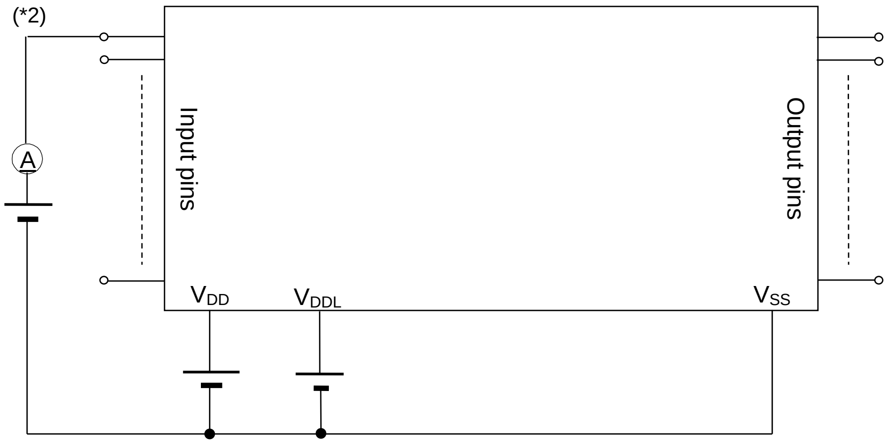
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 3



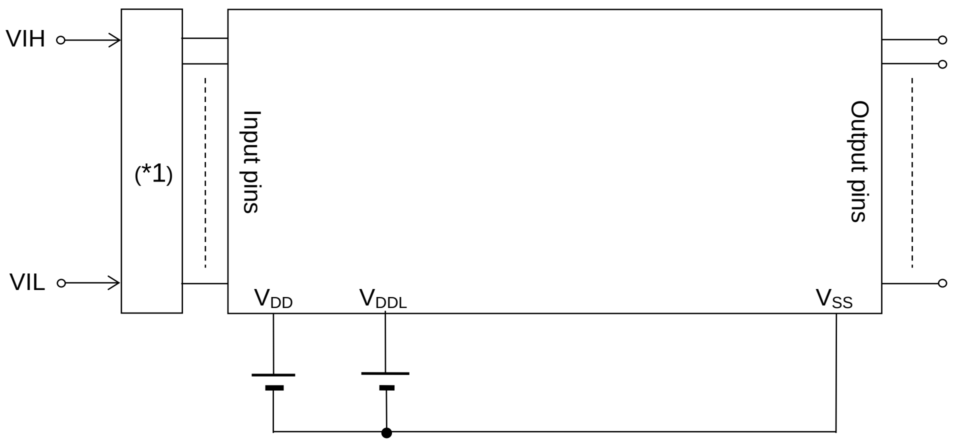
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 4



(*2) Measured connecting specified pins

Measuring circuit 5

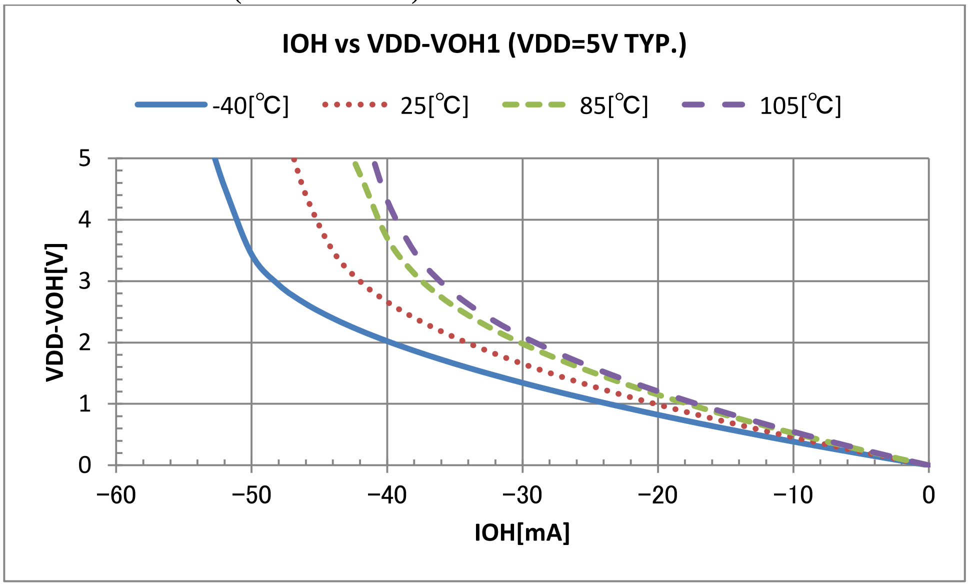


(*1) Input logic circuit to determine the specified measuring conditions

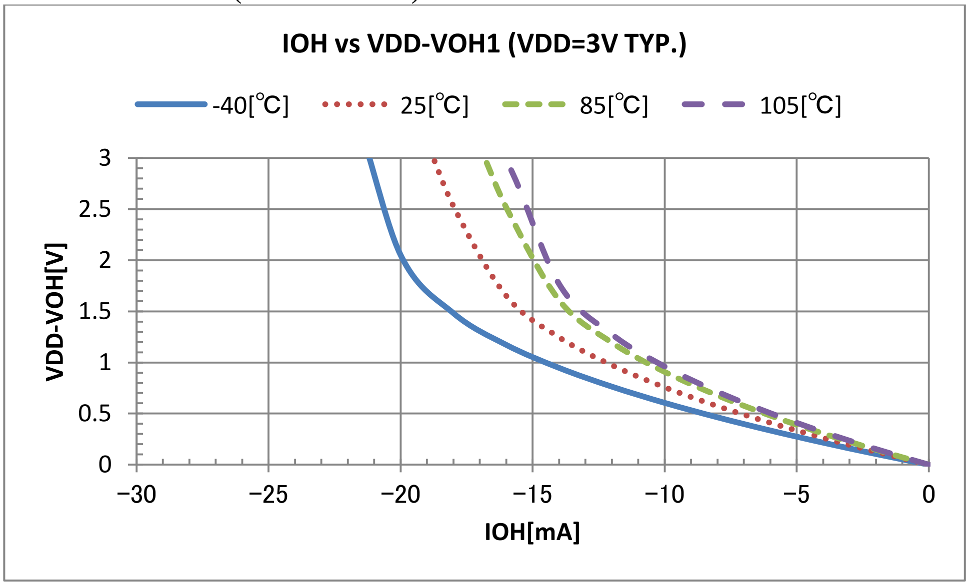
Characteristics graphs

These Graphs on the following pages are references for designing an application.

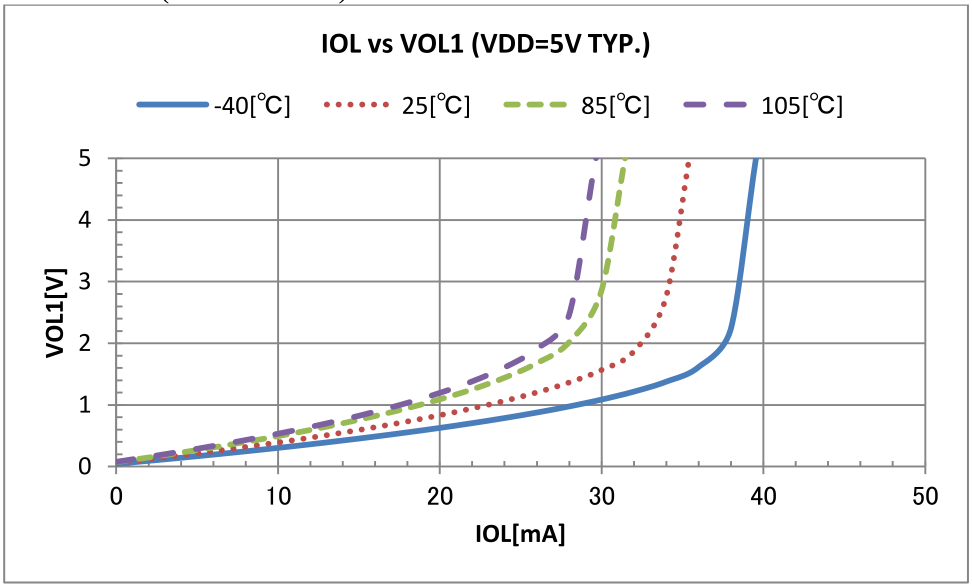
IOH vs VDD-VOH1 (VDD=5V TYP.)



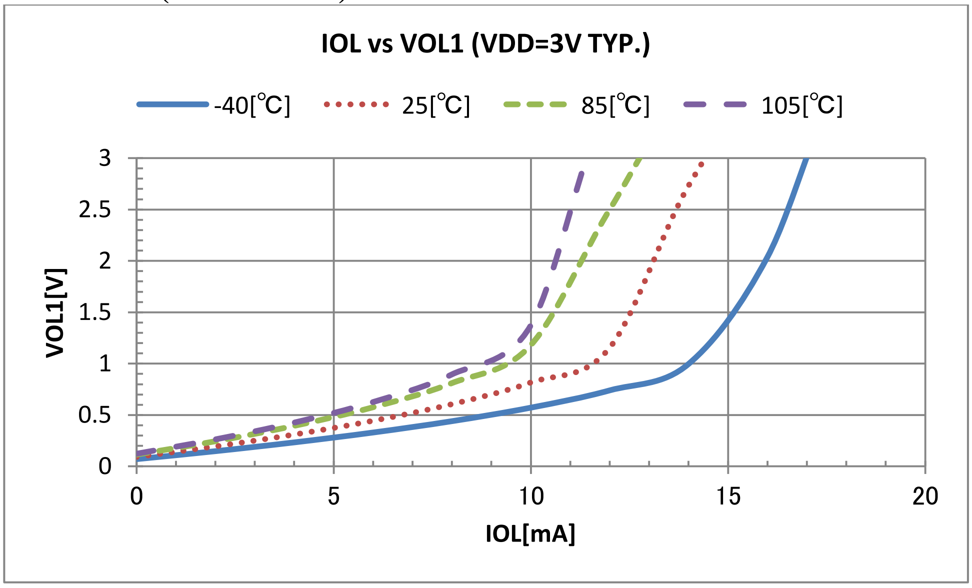
IOH vs VDD-VOH1 (VDD=3V TYP.)



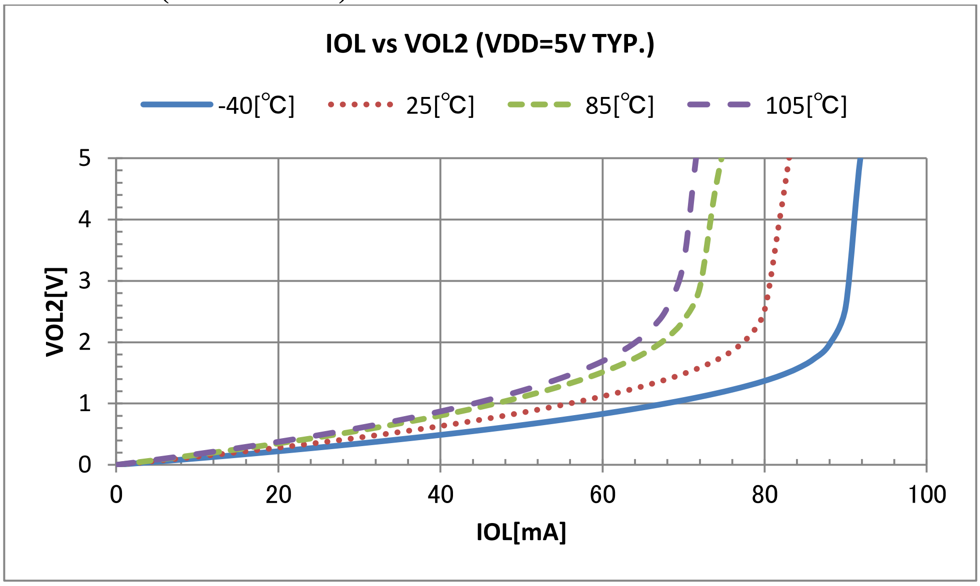
IOL vs VOL1 (VDD=5V TYP.)



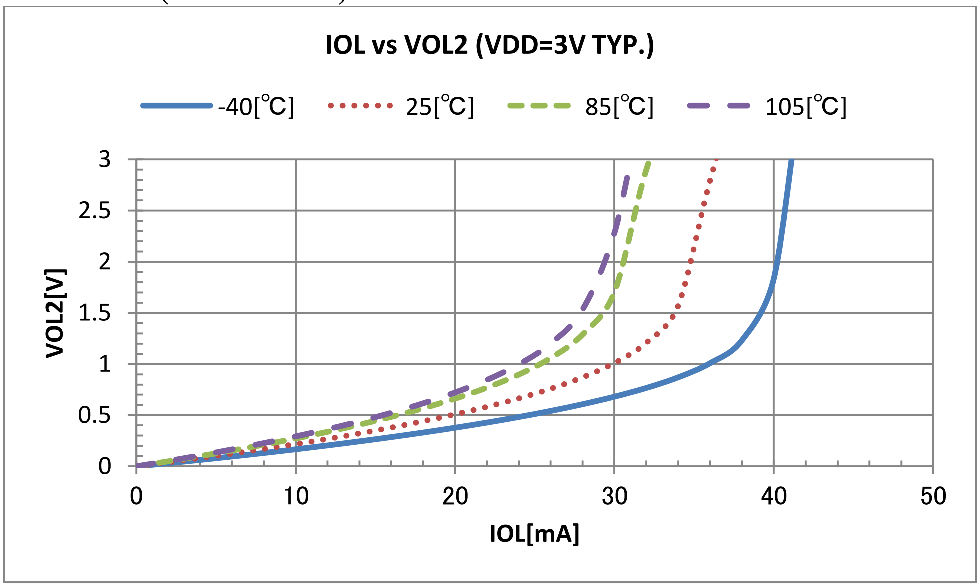
IOL vs VOL1 (VDD=3V TYP.)



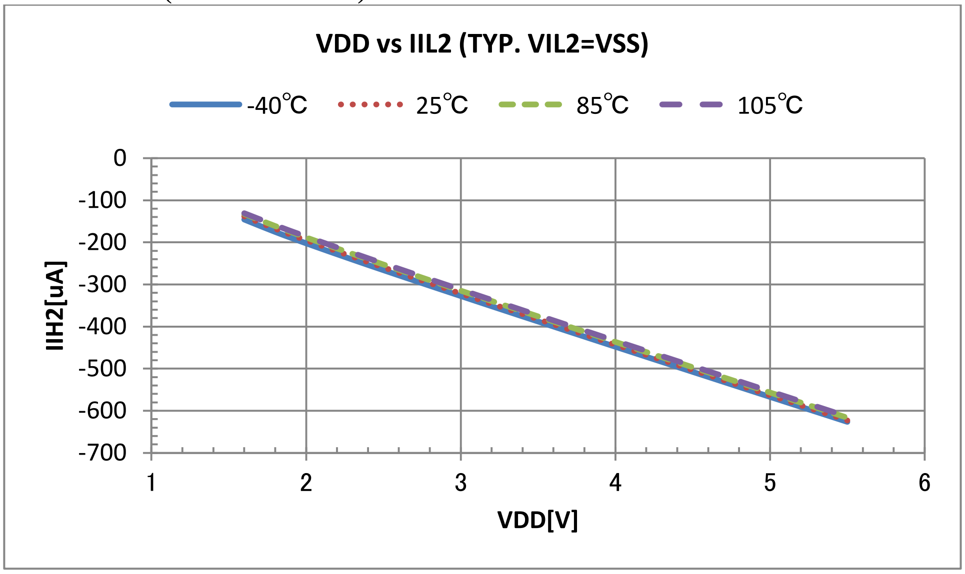
IOL vs VOL2 (VDD=5V TYP.)



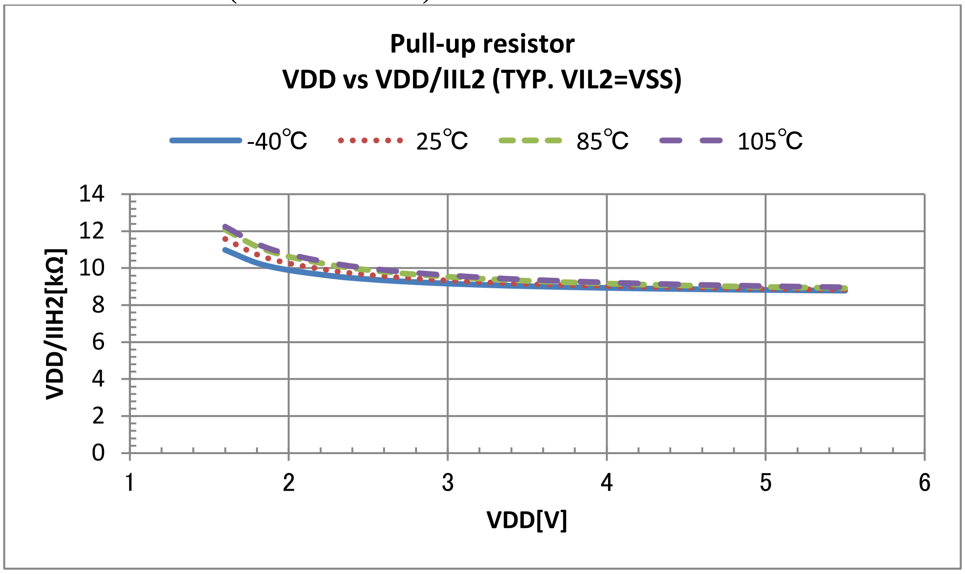
IOL vs VOL2 (VDD=3V TYP.).



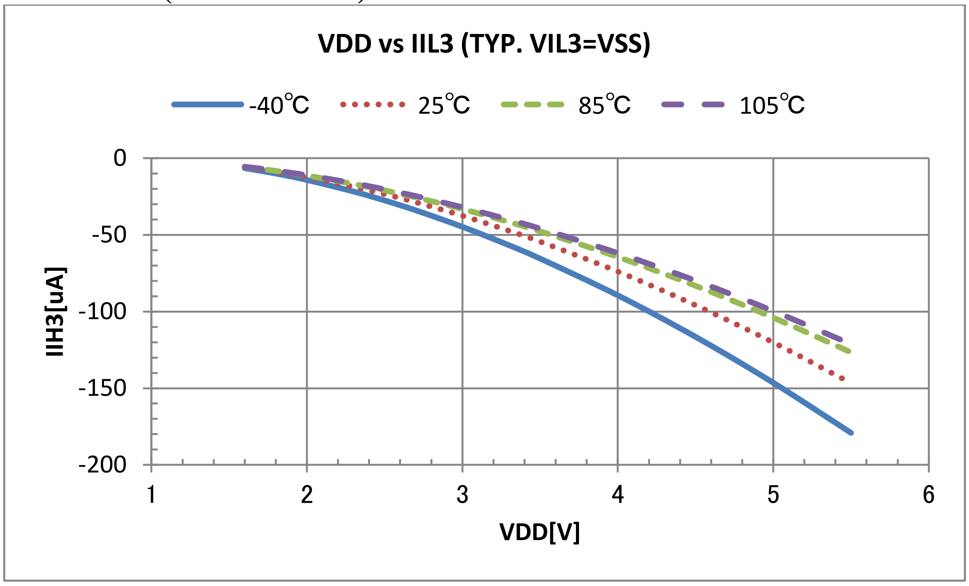
VDD VS IIL2 (TYP. VIL2=VSS)



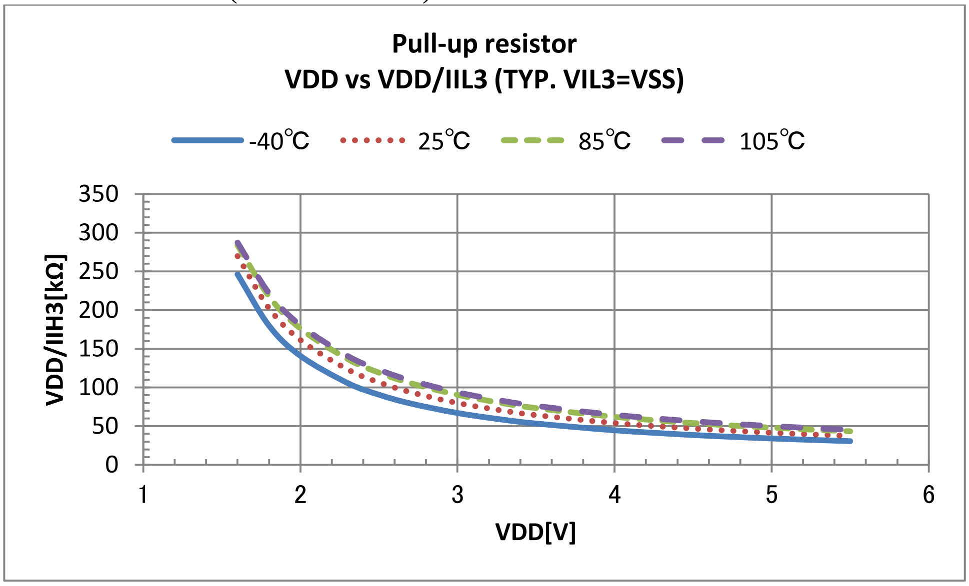
Pull-up resistor
VDD VS VDD/IIL2 (TYP. VIL2=VSS)



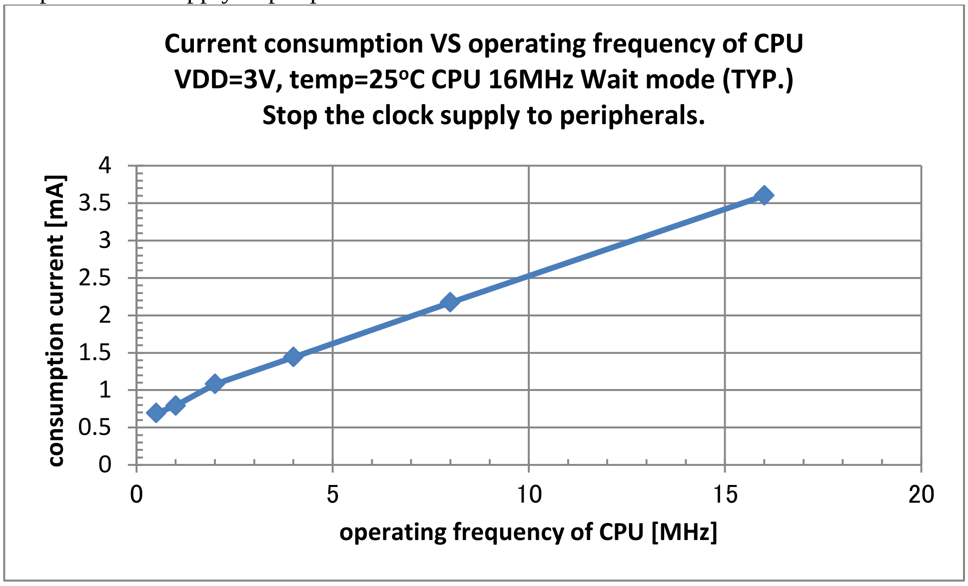
VDD VS IIL3 (TYP. VIL3=VSS)



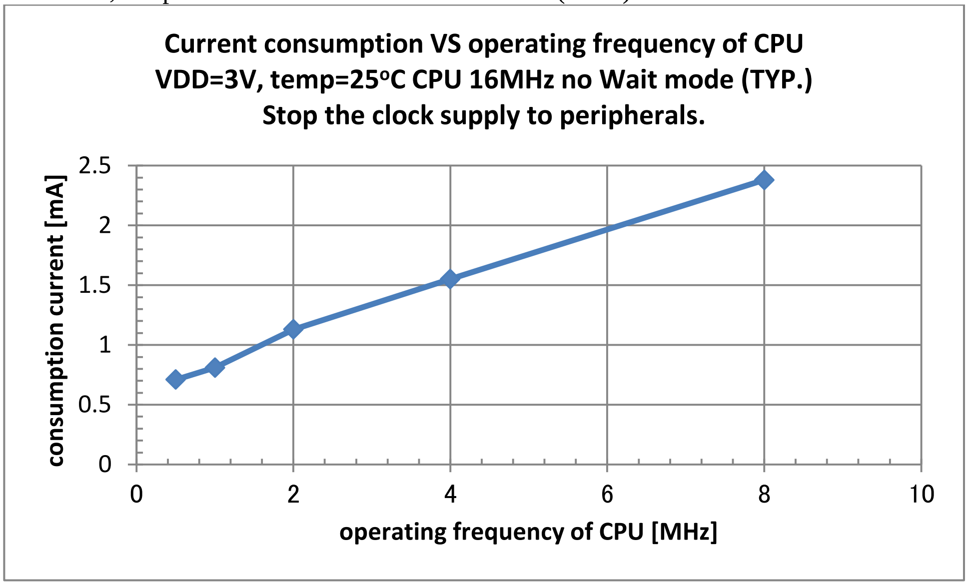
Pull-up resistor
VDD VS VDD/IIL3 (TYP. VIL3=VSS)



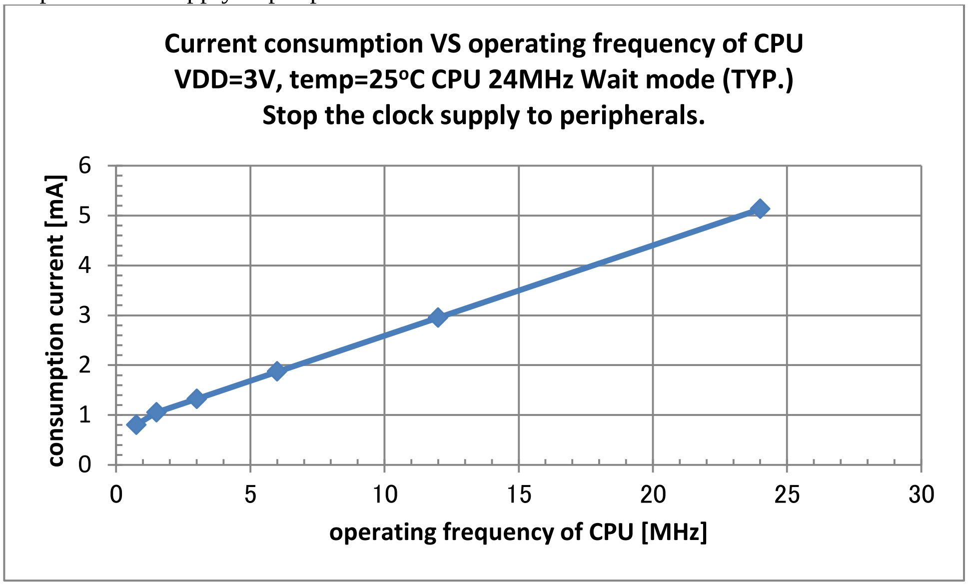
Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



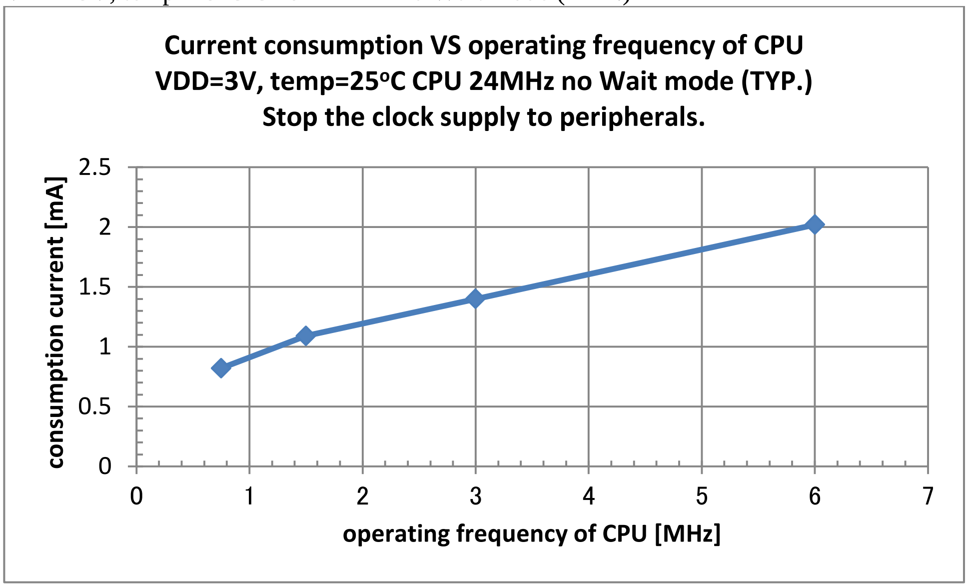
VDD=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)



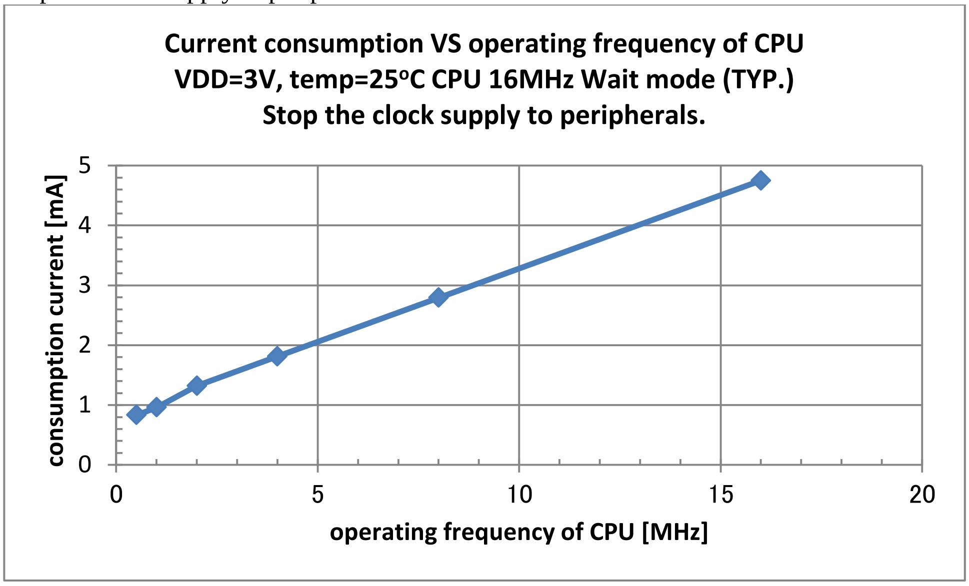
Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



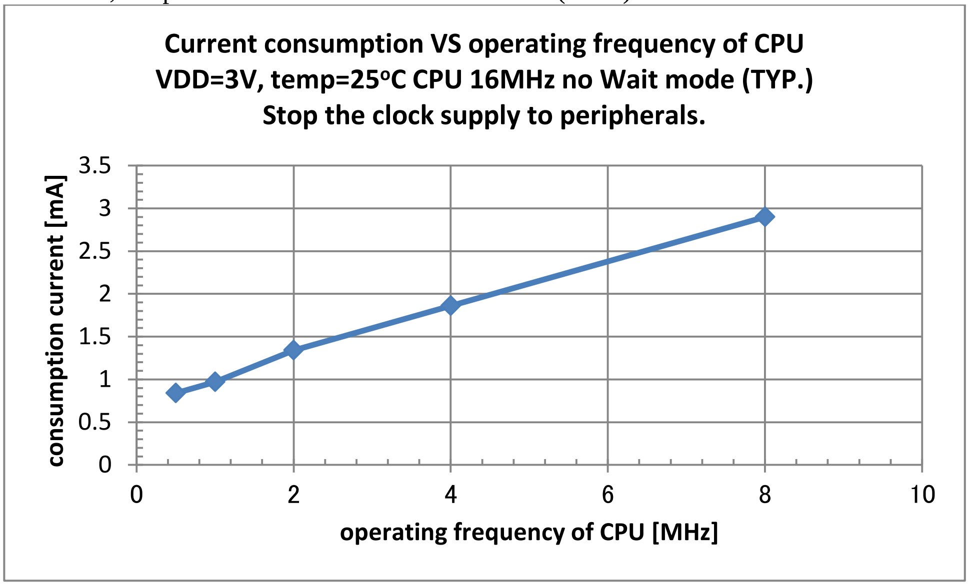
VDD=3V, temp=25°C CPU 24MHz no Wait mode (TYP.)



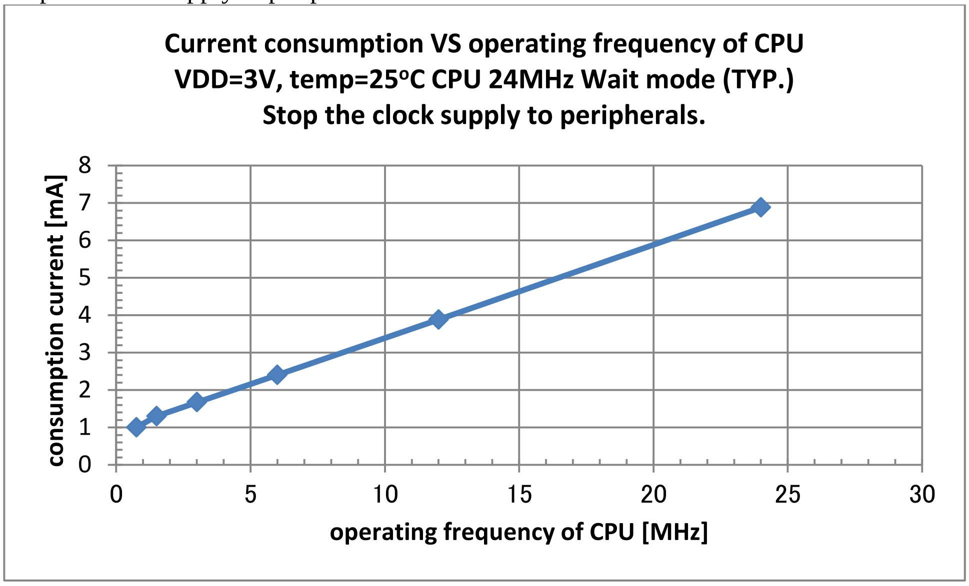
Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



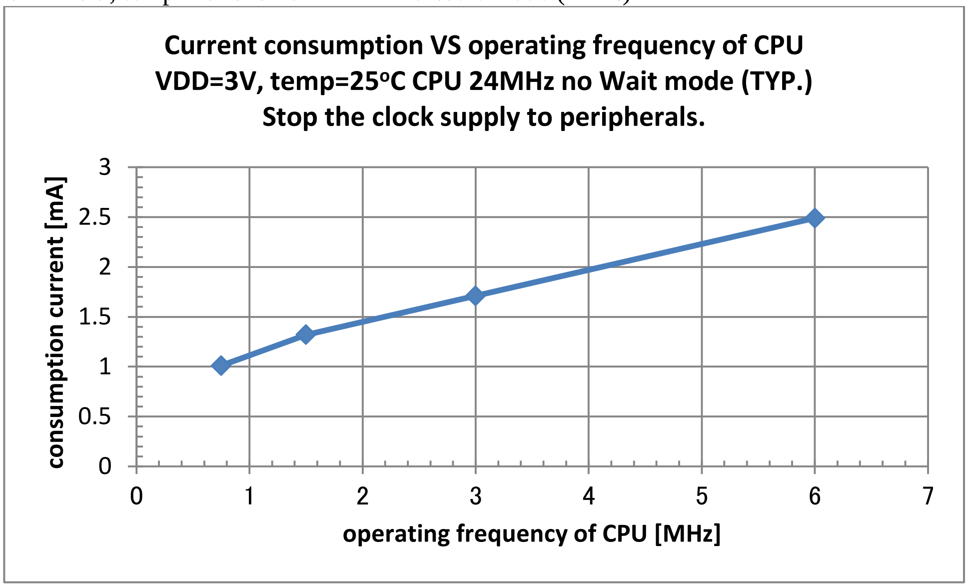
VDD=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)



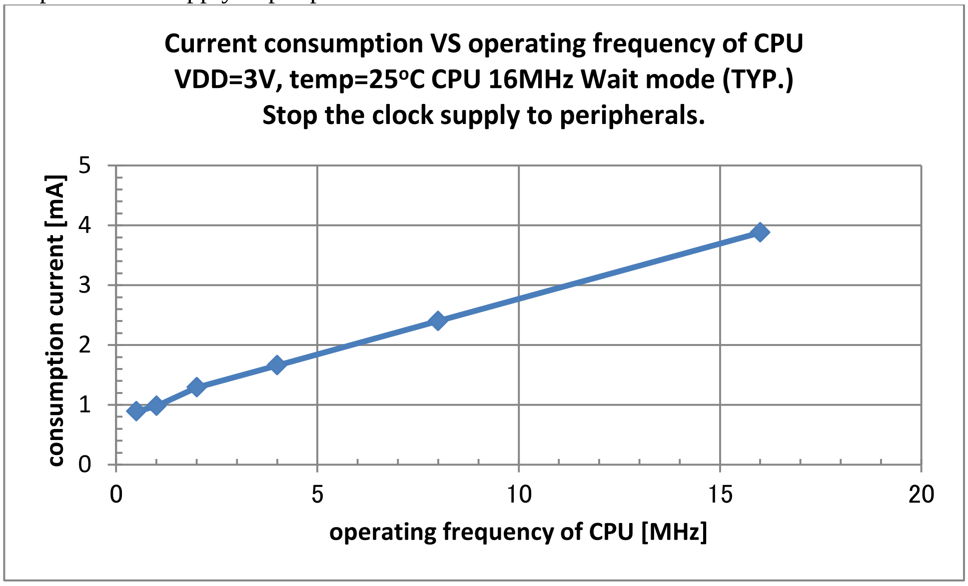
Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



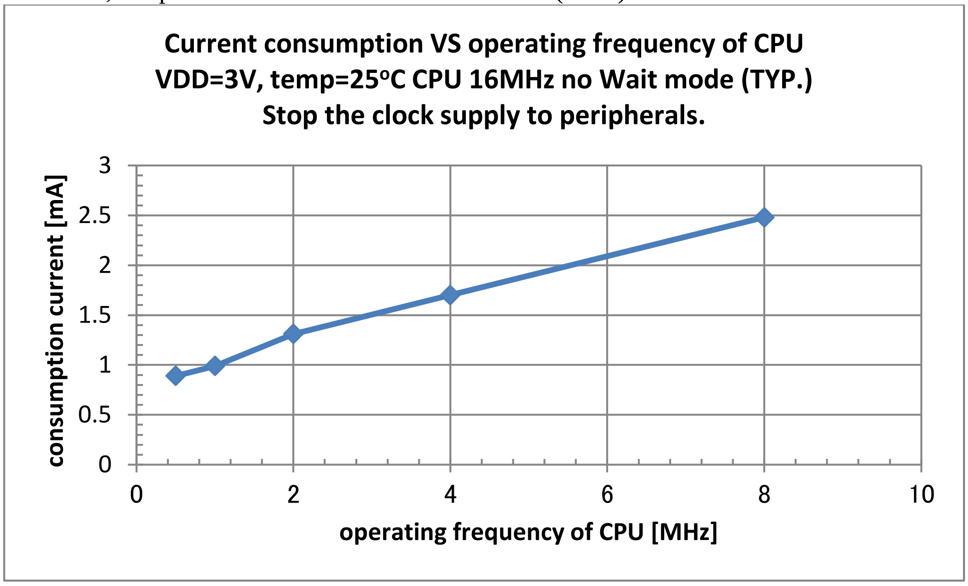
VDD=3V, temp=25°C CPU 24MHz no Wait mode (TYP.)



Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 16MHz Wait mode (TYP.)
Stop the clock supply to peripherals.

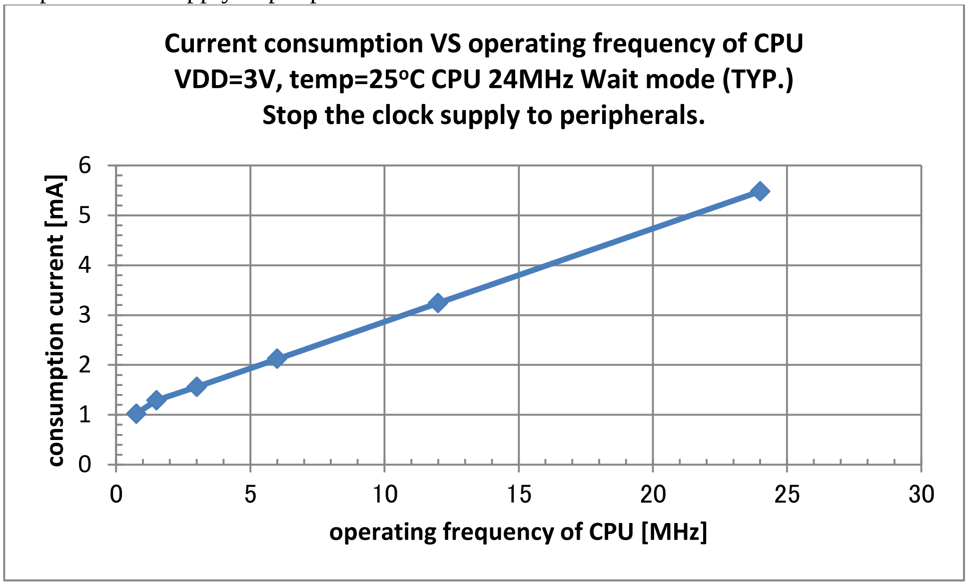


VDD=3V, temp=25°C CPU 16MHz no Wait mode (TYP.)

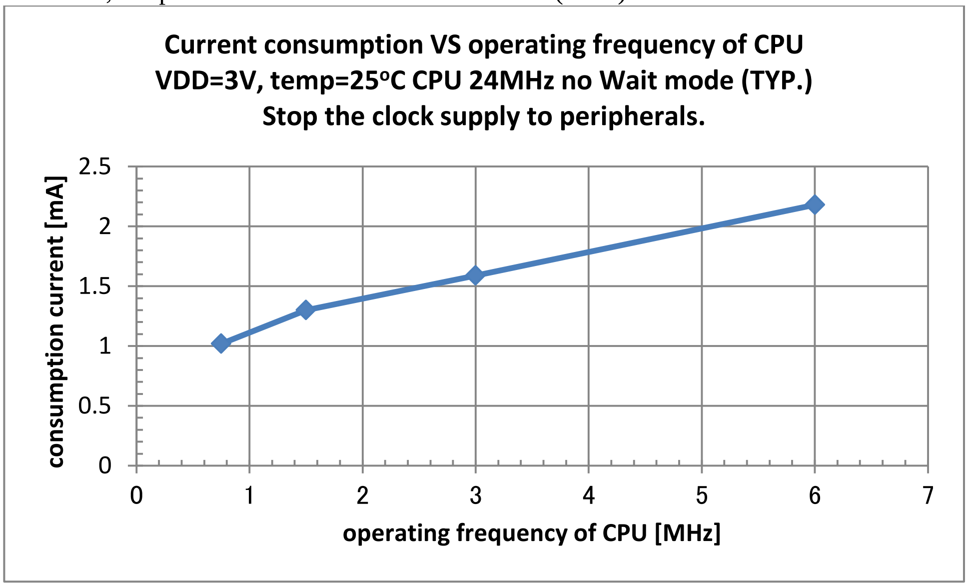


Product: ML62Q1558, ML62Q1559, ML62Q1568, ML62Q1569, ML62Q1578, ML62Q1579

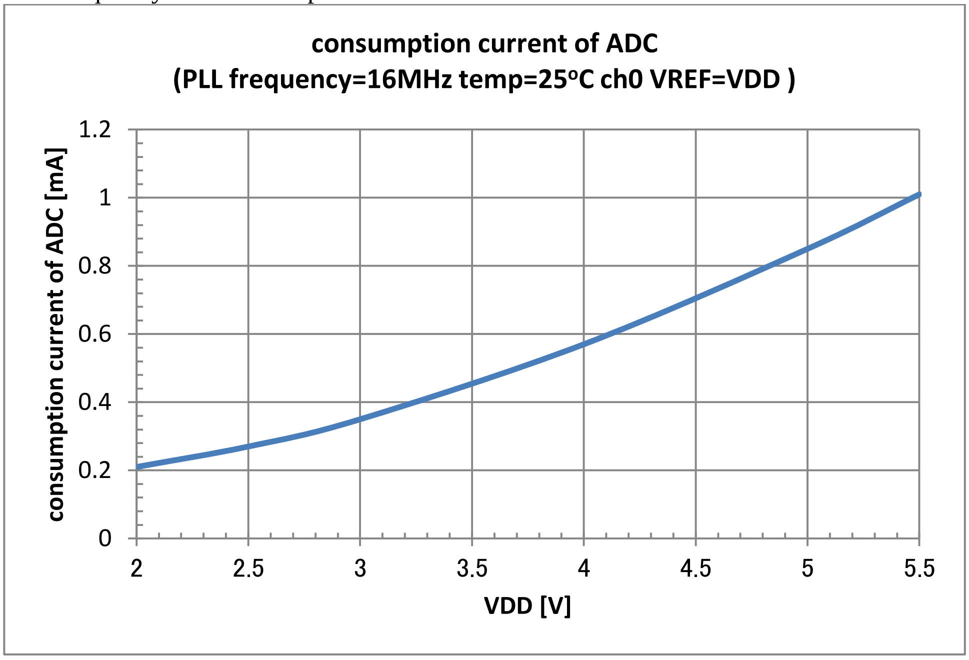
Current consumption VS operating frequency of CPU
VDD=3V, temp=25°C CPU 24MHz Wait mode (TYP.)
Stop the clock supply to peripherals.



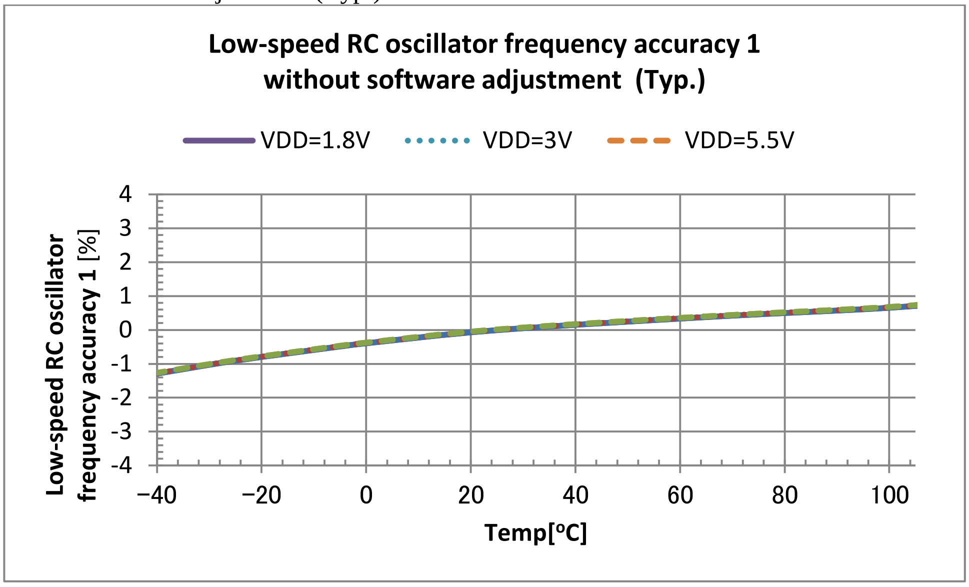
VDD=3V, temp=25°C CPU 24MHz no Wait mode (TYP.)



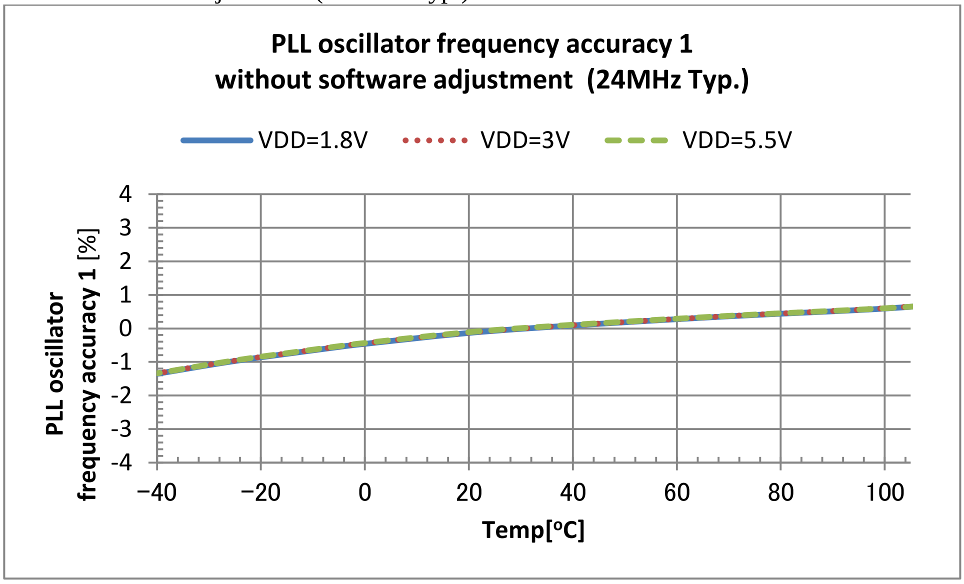
Consumption current of ADC VS operating voltage
PLL frequency=16MHz temp=25°C ch0 VREF=VDD



TEMP VS Low-speed RC oscillator frequency accuracy 1
without software adjustment (Typ.)

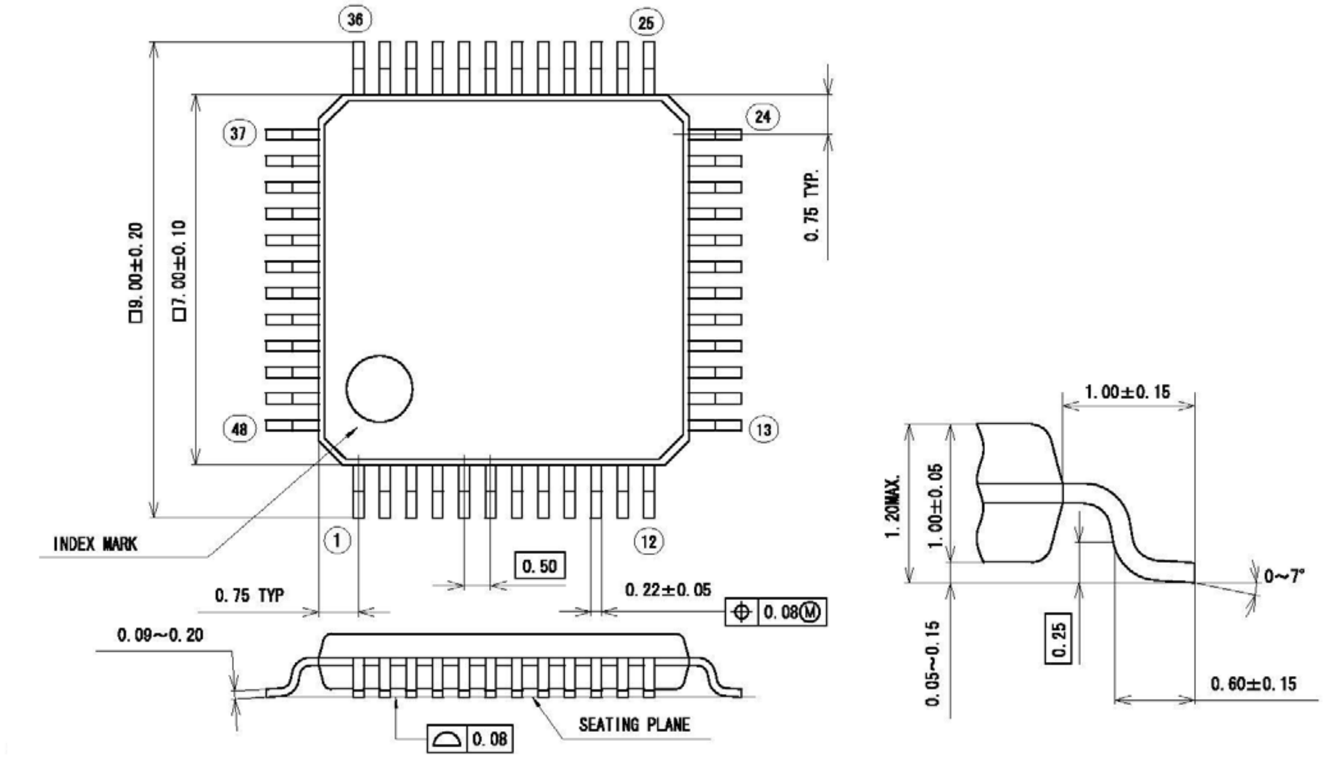


TEMP VS PLL oscillator frequency accuracy 1
without software adjustment (24MHz Typ.)



PACKAGE DIMENSIONS

48pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

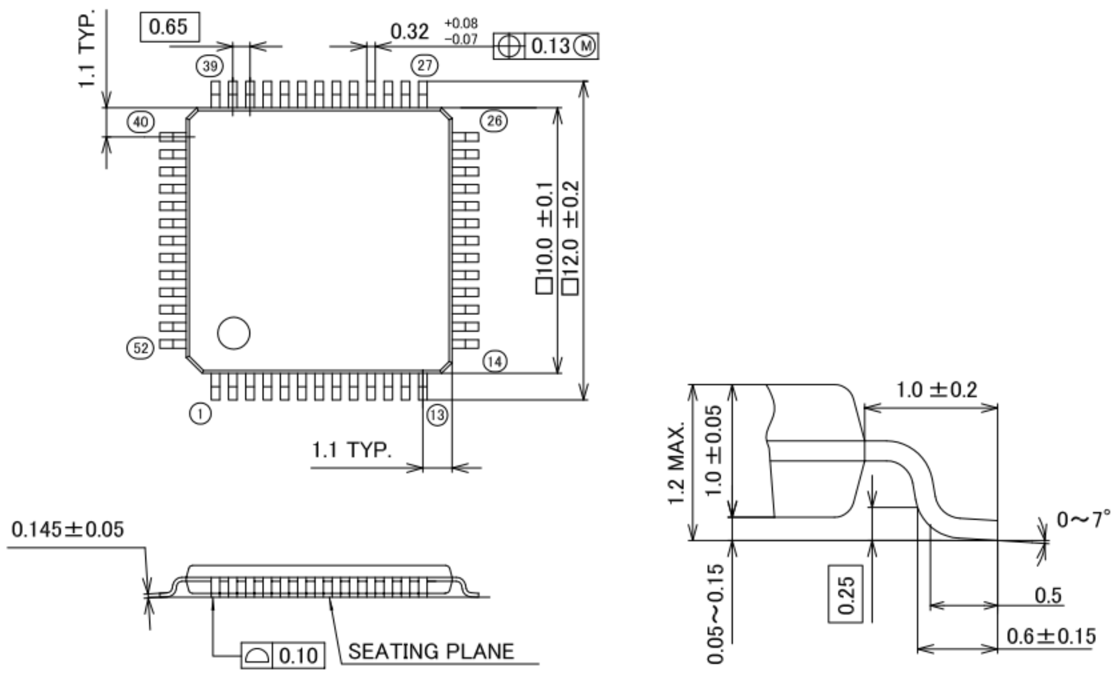
LAPIS Semiconductor Co., Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	3
PLATING THICKNESS	MORE THAN 6 μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/14/2014

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

52pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION,DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

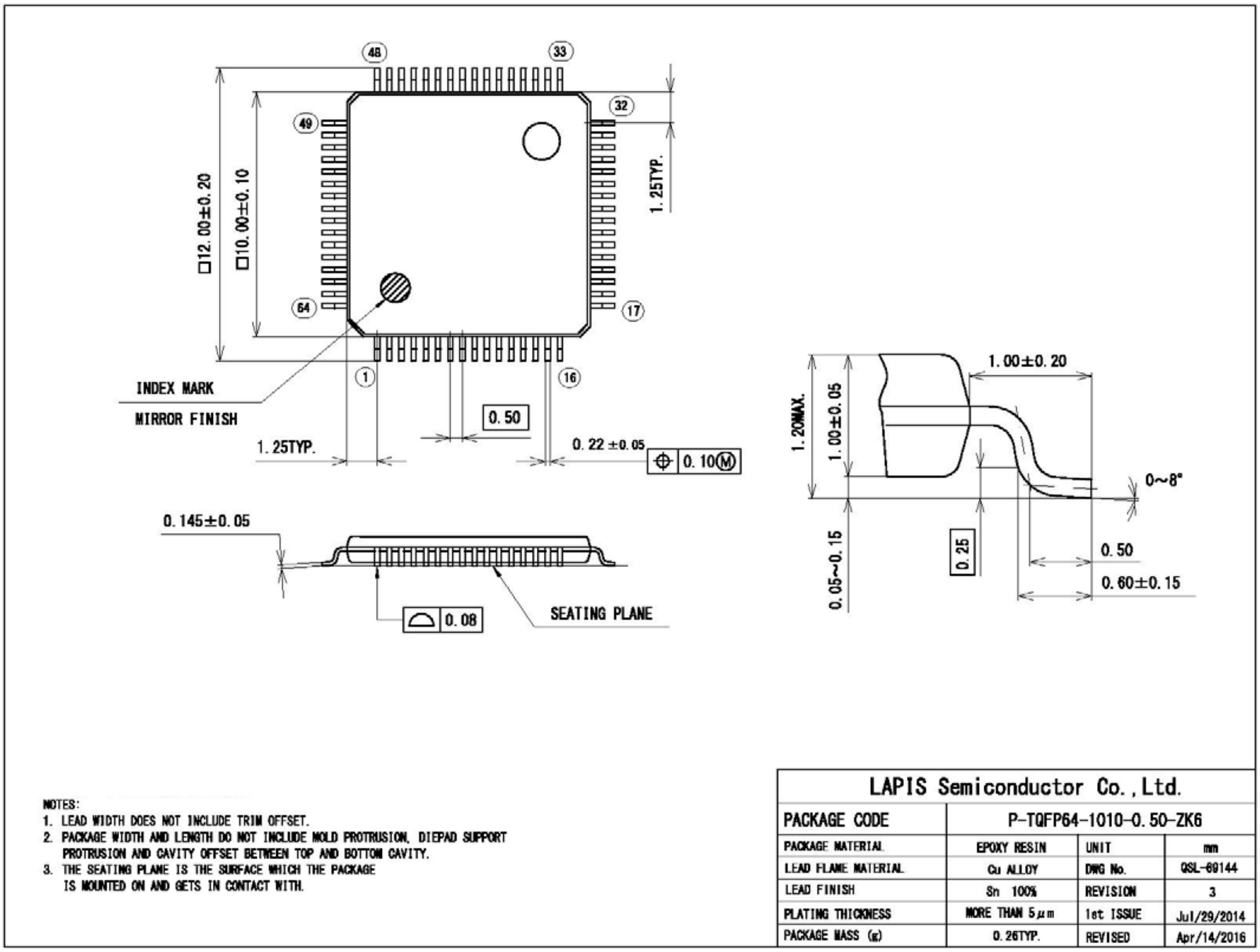
LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP52-1010-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69380
LEAD FINISH	Sn	REVISION	1
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Dec/21/2016
PACKAGE MASS (g)	0.28TYP.	REVISED	

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin TQFP Package

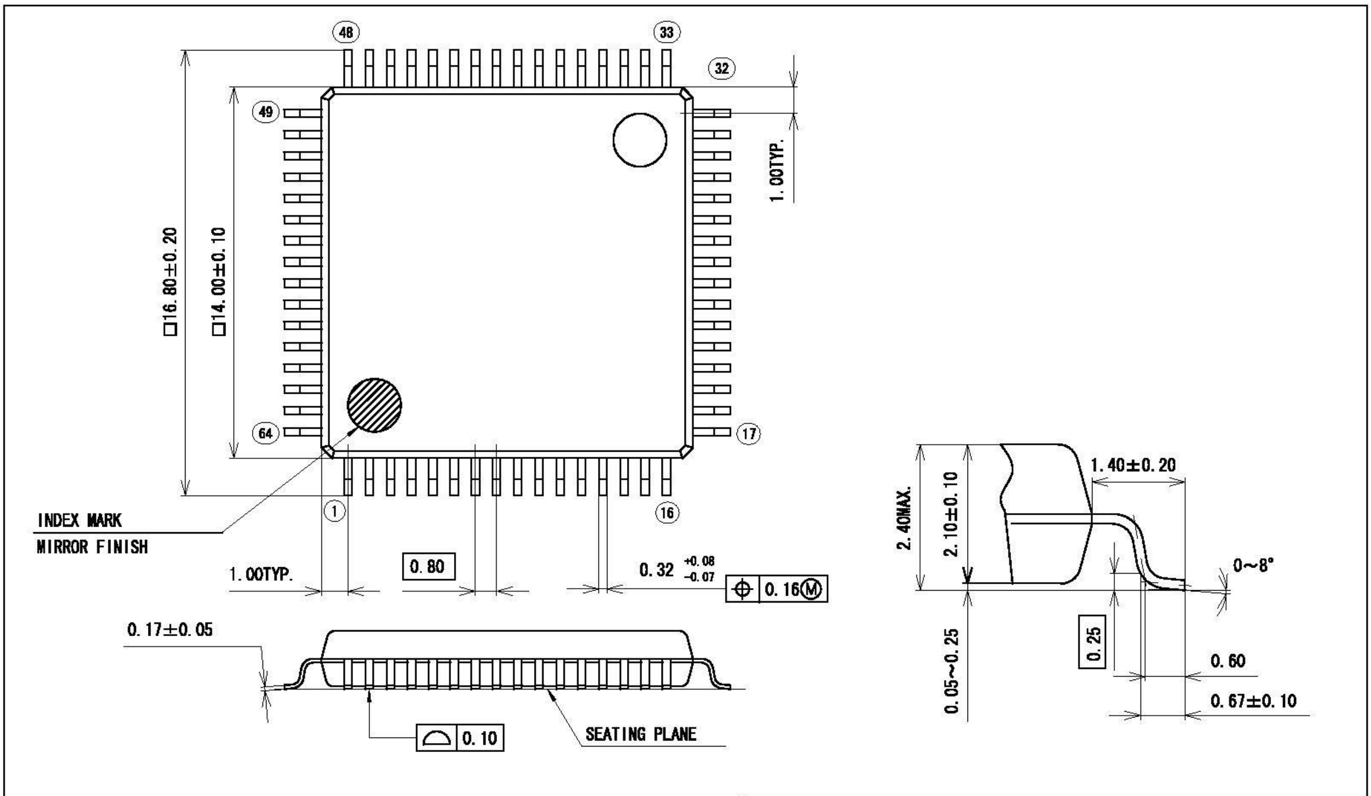


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin QFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

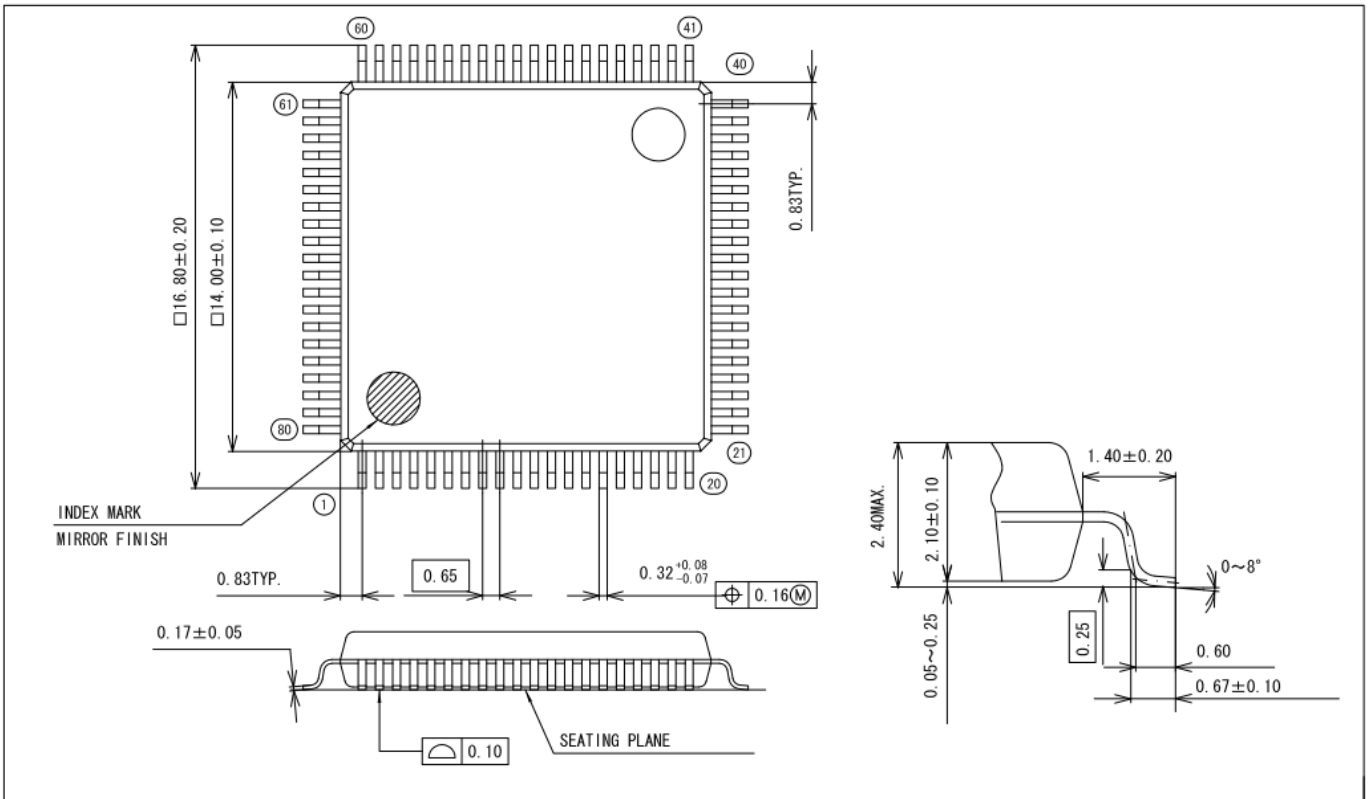
LAPIS Semiconductor Co., Ltd.			
PACKAGE CODE	P-QFP64-1414-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69124
LEAD FINISH	Sn 100%	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.87TYP.	REVISED	

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

80pin QFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

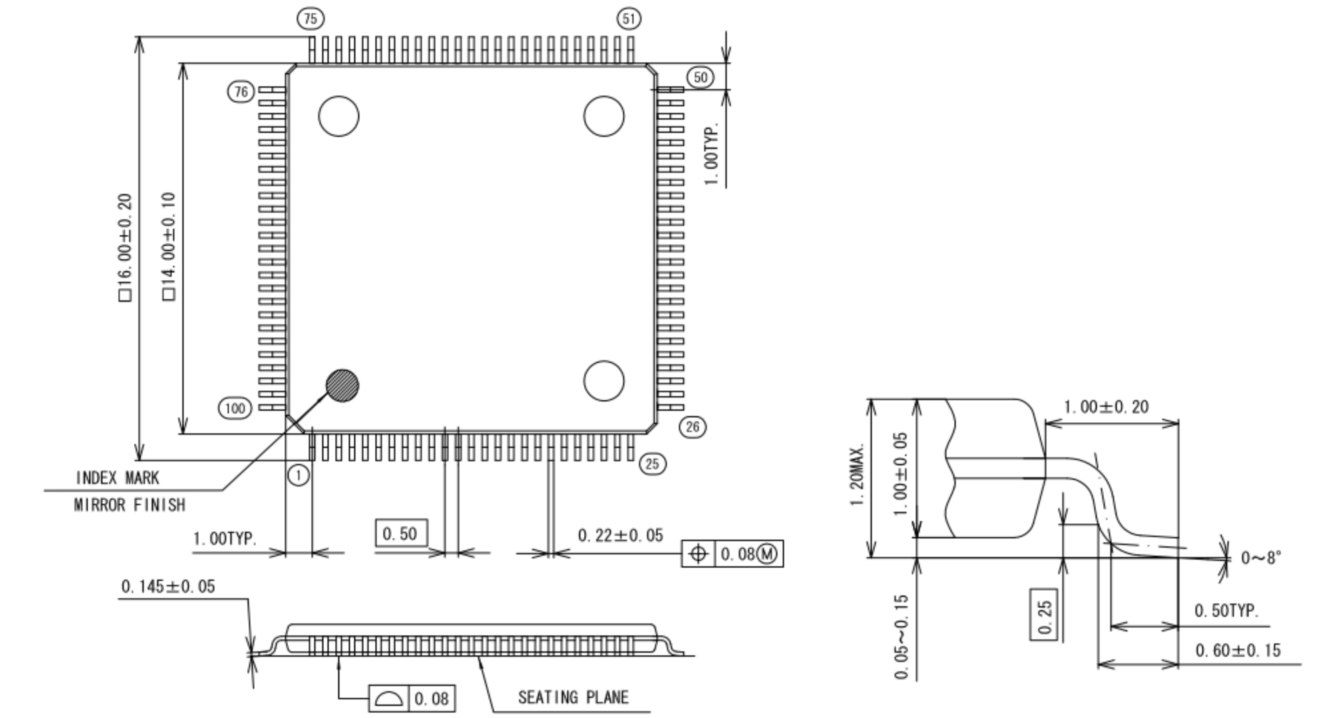
LAPIS Semiconductor Co., Ltd.			
PACKAGE CODE	P-QFP80-1414-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69125
LEAD FINISH	Sn 100%	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.85TYP	REVISED	

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

100pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

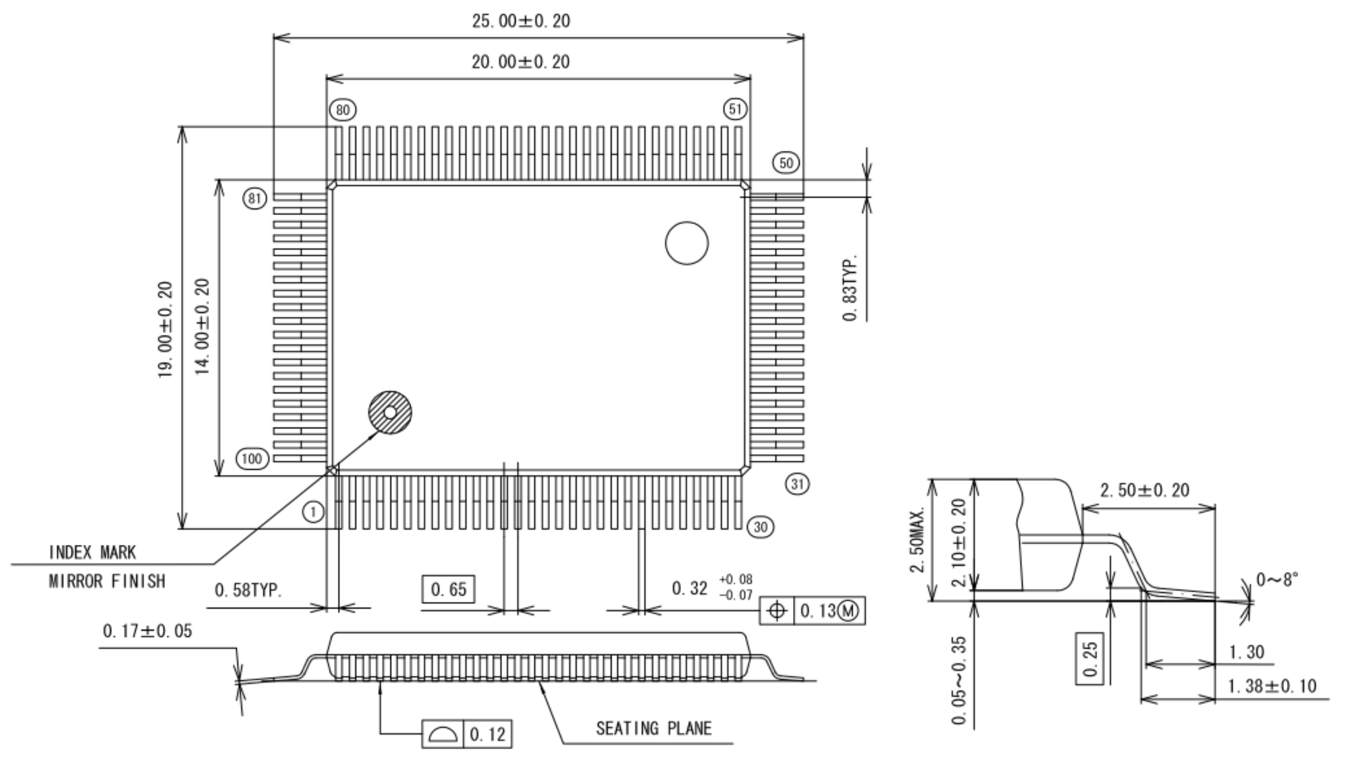
LAPIS Semiconductor Co., Ltd.			
PACKAGE CODE	P-TQFP100-1414-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69147
LEAD FINISH	Sn 100%	REVISION	1
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.55TYP.	REVISED	

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

100pin QFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co., Ltd.			
PACKAGE CODE	P-QFP100-1420-0.65-BK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	42ALLOY	DWG No.	QSL-68760
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	May/10/2012
PACKAGE MASS (g)	1.29TYP.	REVISED	Jul/30/2014

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

<table>
<tr><th rowspan="2">Document No.</th><th rowspan="2">Date</th><th colspan="2">Page</th><th rowspan="2">Description</th></tr>
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<tr><td>FEDL62Q1500-01</td><td>Dec 17, 2018</td><td>-</td><td>-</td><td>1st Revision.</td></tr>
<tr><td rowspan="2">FEDL62Q1500-02</td><td rowspan="2">Jan 9, 2019</td><td>1</td><td>1</td><td>Changed the products under developing (Table 1 ML62Q1500 Group Product List)</td></tr>
<tr><td>26</td><td>26</td><td>Deleted “(TBD)” of Current Consumption 1</td></tr>
<tr><td rowspan="6">FEDL62Q1500-03</td><td rowspan="6">May 15, 2019</td><td>1</td><td>1</td><td>Changed the products under developing (Table 1 ML62Q1500 Group Product List)</td></tr>
<tr><td>28</td><td>28</td><td>Updated Current Consumption 3</td></tr>
<tr><td>32</td><td>32</td><td>Added comment “*6” to the IOHL.</td></tr>
<tr><td>52</td><td>52</td><td>Updated 16MHz Characteristics graphs</td></tr>
<tr><td>53,55</td><td>53,55</td><td>Updated 24MHz Characteristics graphs</td></tr>
<tr><td>-</td><td>56,57</td><td>Added ML62Q1558/ML62Q1559/ML62Q1568/ML62Q1569/ ML62Q1578/ML62Q1579 Current consumption VS operating frequency of CPU</td></tr>
<tr><td rowspan="3">FEDL62Q1500-04</td><td rowspan="3">May 31, 2019</td><td>3,4</td><td>3,4</td><td>Updated the descriptions of DMA and Functional Timer.</td></tr>
<tr><td>25</td><td>25</td><td>Changed I_{OUTH} (total) and I_{OUTL} (total) of Absolute Maximum Ratings to 180mA from 150mA.</td></tr>
<tr><td>32</td><td>32</td><td>Corrected comment of the IOHLs.</td></tr>
</table>

<u>Notes</u>

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